Numonyx™ Axcell™ M29EW Datasheet

256-Mbit, 512-Mbit, 1-Gbit, 2-Gbit (x8/x16, uniform block)
3 V supply flash memory

Features

- Supply voltage
  - — V_{CC} = 2.7 to 3.6 V for Program, Erase and Read
  - — V_{CCQ} = 1.65 to 3.6 V for I/O buffers
- Asynchronous Random/Page Read
  - — Page size: 16 words or 32 bytes
  - — Page access: 25 ns
  - — Random access: 100ns (Fortified BGA); 110 ns (TSOP)
- Buffer Program
  - — 512-word program buffer
- Programming time
  - — 0.88 µs per byte (1.14MB/s) typical when using full buffer size in buffer program
- Memory organization
  - — Uniform blocks, 128 Kbytes/64 Kwords each
- Program/Erase controller
  - — Embedded byte/word program algorithms
- Program/ Erase Suspend and Resume
  - — Read from any block during Program Suspend
  - — Read and Program another block during Erase Suspend
- Unlock Bypass/Block Erase/Chip Erase/Write to Buffer
  - — Faster Buffered/Batch Programming
  - — Faster Block and Chip Erase
- Vpp/WP# pin protection
  - — Protects first or last block regardless of block protection settings
- Software protection
  - — Volatile Protection
  - — Non-Volatile Protection
  - — Password Protection
  - — Password Access
- Extended Memory block
  - — 128-word/256-byte block for permanent, secure identification.
  - — can be programmed and locked by factory or by the customer
- Low power consumption
  - — Standby and automatic standby
- Minimum 100,000 Program/Erase cycles per block
- ETOX™* X (65nm) MLC technology
- Fortified BGA and TSOP packages
- JESD47E Compliant
- Green packages available
  - — RoHS Compliant
  - — Halogen Free

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1 Description

The Numonyx™ Axcell™ M29EW flash memory based on 65nm MLC technology is the world's leading line of parallel NOR flash for embedded applications. It can be read, erased and reprogrammed; and these operations can be performed using a single low voltage (2.7 to 3.6 V) supply. Upon power-up, the memory defaults to its array read mode.

The main memory array is divided into 64-Kword/128-Kbyte uniform blocks that can be erased independently so that valid data can be preserved while old data is purged. Program and Erase commands are written to the command interface of the memory. An on-chip Program/Erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error condition can be identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The M29EW supports Asynchronous Random Read and Page Read from all blocks of the memory array. It also features an internal program buffer which improves throughput by programming 512 words via one command sequence.

The M29EW contains a 128-word Extended Memory Block which overlaps addresses with array block 0. The user can program this additional space; then protect it to permanently secure its contents.

The device features different levels of hardware and software protection to secure blocks from unwanted modification (program or erase):

- Hardware protection:
  - The V_{PP}/WP# provides a hardware protection of either the highest (M29EWH) or the lowest (M29EWL) block of the main memory array.
- Software protection:
  - Volatile Protection
  - Non-Volatile Protection
  - Password Protection
  - Password Access

The M29EW is offered in TSOP56 (14 x 20 mm) and Fortified BGA64 (11 x 13 mm, 1 mm pitch) packages.

The memories are delivered with all the bits erased (set to '1').

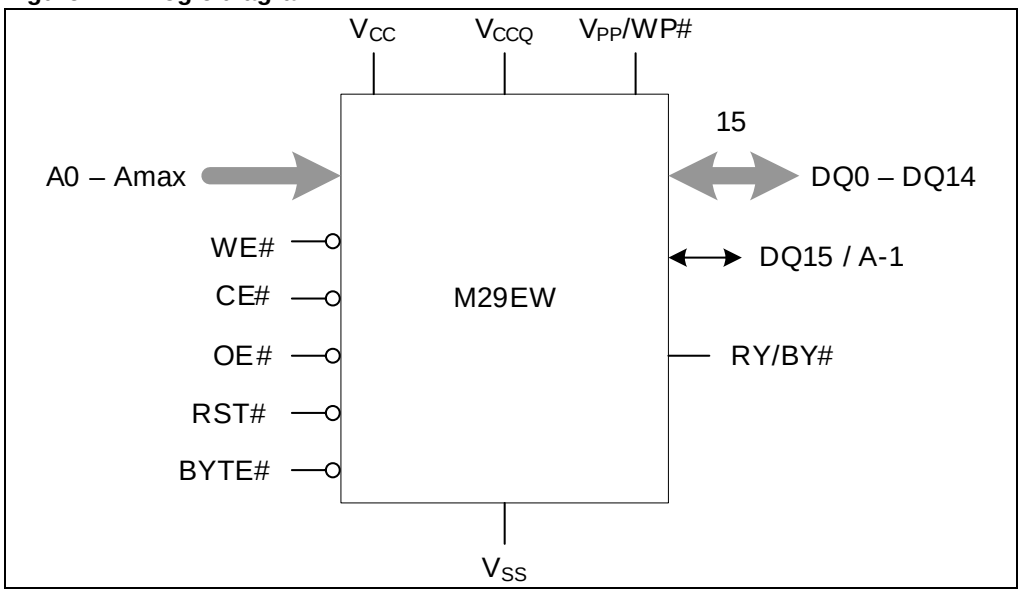
Also see *Appendix B: Common Flash Interface (CFI) on page 110* and *Table 4: Block addresses on page 11* for a full list of the block addresses.

Table 1. Signal Descriptions

Name	Description	Direction
A0-Amax	Address inputs	Inputs
DQ0-DQ7	Data inputs/outputs	I/O
DQ8-DQ14	Data inputs/outputs	I/O
DQ15/A–1	Data input/output or address input	I/O
CE#	Chip Enable	Input
OE#	Output Enable	Input
WE#	Write Enable	Input
RST#	Reset	Input
RY/BY#	Ready/Busy output	Output
BYTE#	Byte/word organization select	Input
V_{CCQ}	Input/output buffer supply voltage	Supply
V_{CC}	Supply voltage	Supply
V_{PP}/WP#(1)	V_{PP}/Write Protect	Input
V_{SS}	Ground	-
NC	Not connected	-

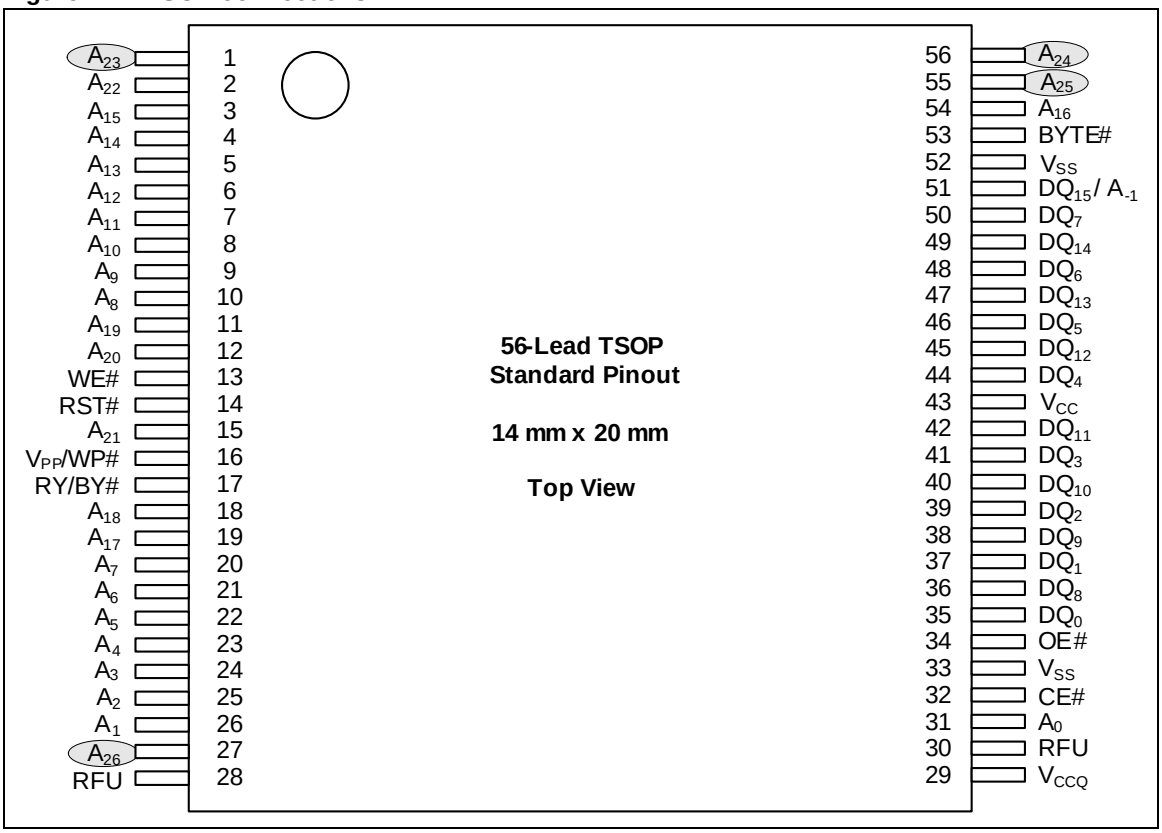
1. V_{PP}/WP# may be left unconnected as it is internally connected to a pull-up resistor, which enables Program/Erase operations.

Figure 1. Logic diagram



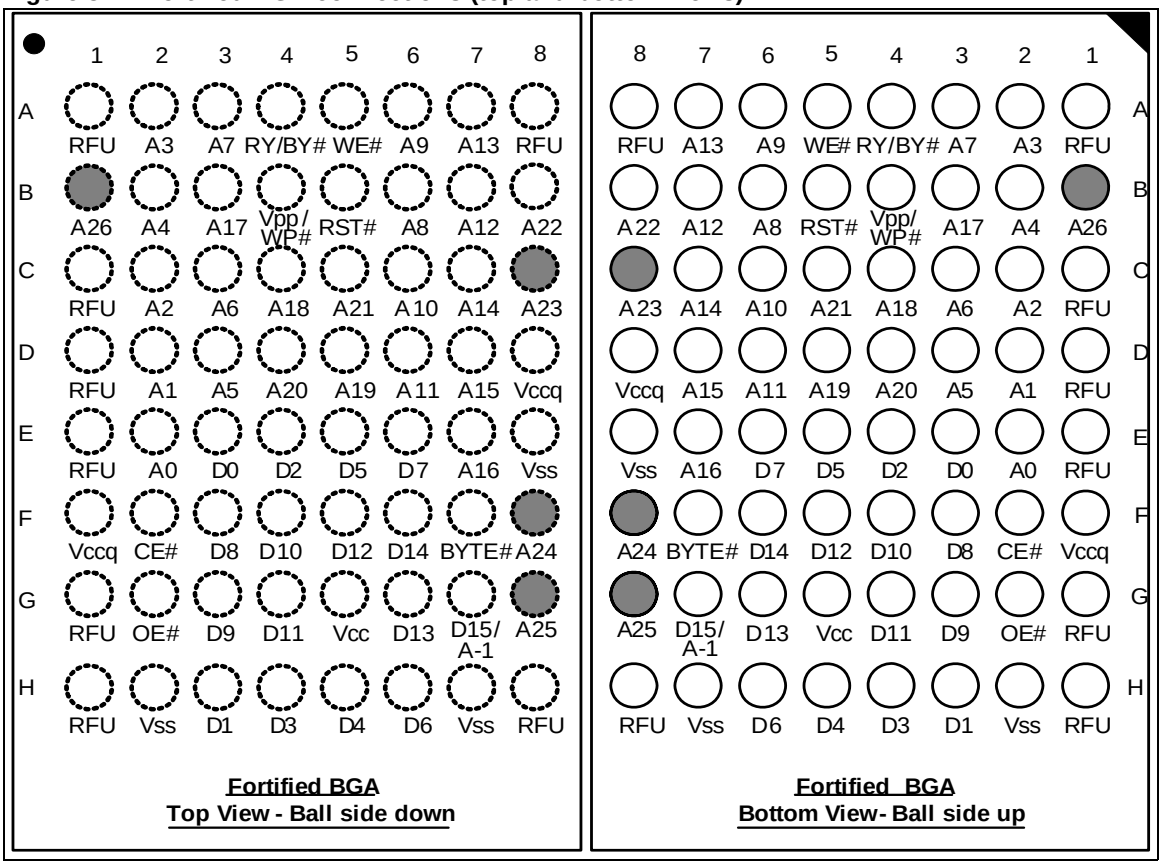
1. A23 is valid for 256-Mbit density and above; otherwise, it is a RFU.
2. A24 is valid for 512-Mbit density and above; otherwise, it is a RFU.
3. A25 is valid for 1-Gbit density and above; otherwise, it is a RFU.
4. A26 is valid for 2-Gbit (1-Gbit/1-Gbit stack) density only; otherwise it's a RFU.
5. RFU stands for Reserved for Future Use and should be not connect.

Figure 2. TSOP connections



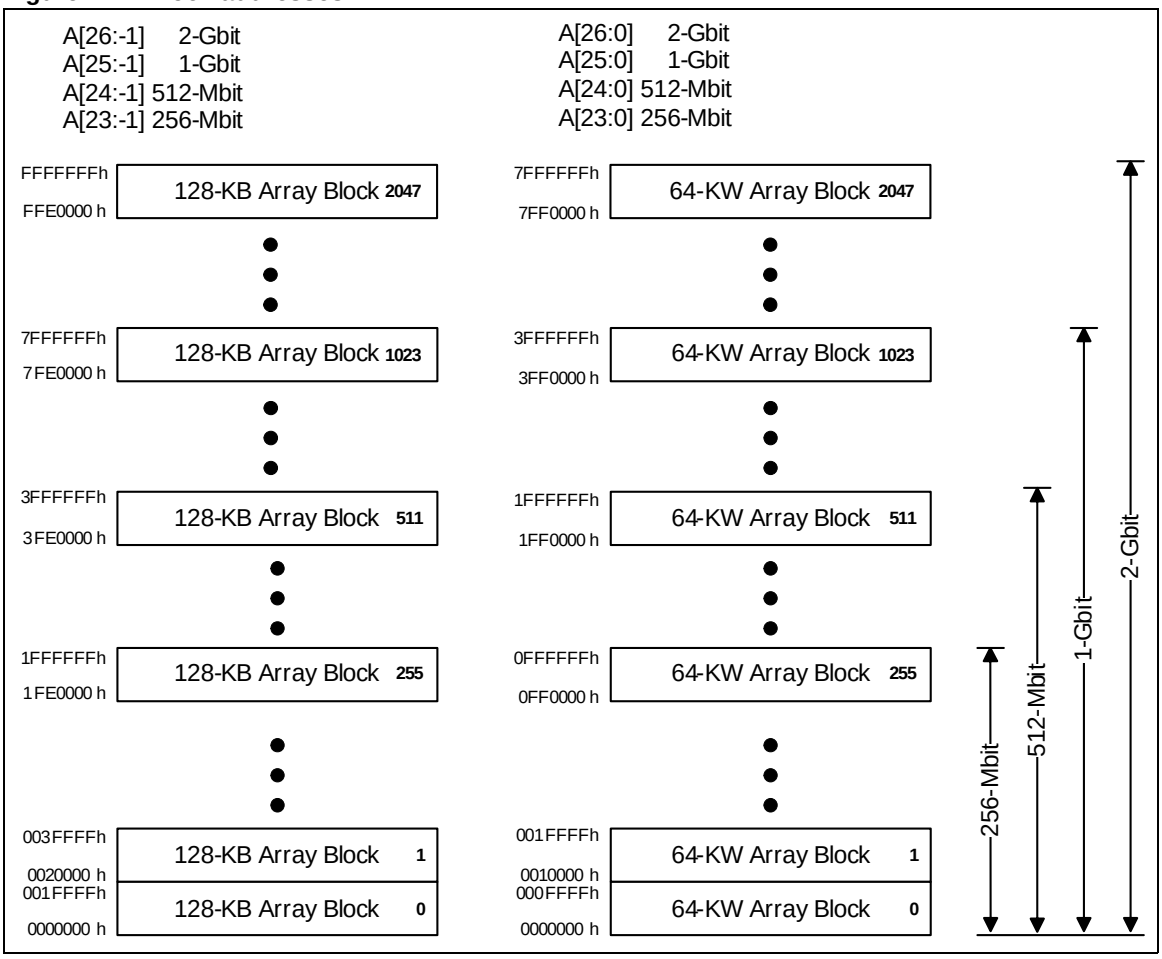
1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256-Mbit density and above; otherwise, it is a RFU.
3. A24 is valid for 512-Mbit density and above; otherwise, it is a RFU.
4. A25 is valid for 1-Gbit density and above; otherwise, it is a RFU.
5. A26 is valid for 2-Gbit (1-Gbit/1-Gbit stack) density only; otherwise it's a RFU.
6. RFU stands for Reserved for Future Use and should be not connect.

Figure 3. Fortified BGA connections (top and bottom views)



1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256-Mbit density and above; otherwise, it is a RFU.
3. A24 is valid for 512-Mbit density and above; otherwise, it is a RFU.
4. A25 is valid for 1-Gbit density and above; otherwise, it is a RFU.
5. A26 is valid for 2-Gbit (1-Gbit/1-Gbit stack) density only; otherwise it's a RFU.
6. RFU stands for Reserved for Future Use and should be not connect.

Figure 4. Block addresses



2 Signal Descriptions

See *Figure 1: Logic diagram*, and *Table 1: Signal Descriptions*, for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-Amax)

The Address inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the command interface of the Program/Erase controller.

2.2 Data inputs/outputs (DQ0-DQ7)

The Data I/O outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the command interface of the internal state machine.

2.3 Data inputs/outputs (DQ8-DQ14)

The Data I/O outputs the data stored at the selected address during a Bus Read operation when BYTE# is High, V_{IH}. When BYTE# is Low, V_{IL}, these pins are not used and are high impedance. During Bus Write operations the Command Register does not use these bits. When reading the Status Register these bits should be ignored.

2.4 Data input/output or address input (DQ15/A–1)

When the device operates in x16 bus mode, this pin behaves as a Data input/output pin, together with DQ8-DQ14. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address. Throughout the text consider references to the Data input/output to include this pin when the device operates in x16 bus mode and references to the Address inputs to include this pin when the device operates in x8 bus mode except when stated explicitly otherwise.

2.5 Chip Enable (CE#)

The Chip Enable pin, CE#, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

2.6 Output Enable (OE#)

The Output Enable pin, OE#, controls the Bus Read operation of the memory.

2.7 Write Enable (WE#)

The Write Enable pin, WE#, controls the Bus Write operation of the memory's command interface.

2.8 V_{PP}/Write Protect (V_{PP}/WP#)

The V_{PP}/Write Protect pin provides two functions, Write Protect function and the V_{PPH} function, which protect the lowest or highest block and allow the memory to enter unlock bypass mode respectively.

The Write Protect function provides a hardware method of protecting the highest or lowest block (see *Section 1: Description*). When V_{PP}/Write Protect is Low, V_{IL}, the highest or lowest block is protected. Program and Erase operations on this block are ignored while V_{PP}/Write Protect is Low.

When V_{PP}/Write Protect is High, V_{IH}, the memory reverts to the previous protection status of the highest or lowest block. Program and Erase operations can now modify the data in this block unless the block is protected using Block protection.

When V_{PP}/Write Protect is raised to V_{PPH} the memory automatically enters the Unlock Bypass mode (see *Section 6.2.4*).

When V_{PP}/Write Protect returns to V_{IH} or V_{IL} normal operation resumes. See the description of the Unlock Bypass command in the command interface section. The transitions from V_{IH} to V_{PPH} and from V_{PPH} to V_{IH} must be slower than t_{VHVPP} (see *Figure 27: Accelerated program timing waveforms*).

Never raise V_{PP}/Write Protect to V_{PPH} from any mode except Read mode, otherwise the memory may be left in an indeterminate state. A 0.1 µF capacitor should be connected between the VPP/Write Protect pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program (see I_{PP1}, I_{PP2}, I_{PP3}, I_{PP4} in *Table 22: DC characteristics*).

The V_{PP}/Write Protect pin may be left unconnected as it features an internal pull-up resistor.

Note: For 2-Gbit (1-Gbit/1-Gbit stack) device, When VPP/WP# pin is low, both the highest block and the lowest block are hardware-protected, namely block 0 and block 2047.

Refer to *Table 2* for a summary of V_{PP}/WP# functions.

Table 2. V_{PP}/WP# functions

V_{PP}/WP#	Function
V_{IL}	Highest block protected or lowest block protected.(1)
V_{IH}	Highest and lowest block unprotected unless a software protection is activated (see *Section 4: Hardware Protection*).
V_{PPH}	Unlock bypass mode.

1. For 2-Gbit (1-Gbit/1-Gbit stack) device, both the highest block and the lowest block are hardware-protected, namely block 0 and block 2047.

2.9 Reset (RST#)

The Reset pin can be used to apply a Hardware Reset to the memory. A Hardware Reset is achieved by holding Reset Low, V_{IL}, for at least t_{PLPX}. After Reset goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See *Section 2.10: Ready/Busy output (RY/BY#)*, *Table 26: Reset AC characteristics*, *Figure 25* and *Figure 26* for more details.

2.10 Ready/Busy output (RY/BY#)

The Ready/Busy pin is an open-drain output that can be used to identify when the device is performing a program or erase operation. During program or erase operations Ready/Busy is Low, V_{OL} (see *Table 17: Status Register bits*). Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance. See *Table 26: Reset AC characteristics*, *Figure 25* and *Figure 26*.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A low value will then indicate that one, or more, of the memories is busy. The 10Kohm or bigger resistor is recommended as pull-up resistor to achieve 0.1V V_{OL}.

2.11 Byte/Word organization select (BYTE#)

The BYTE# pin is used to switch between the x8 and x16 Bus modes of the memory. When Byte/Word organization select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

2.12 V_{CC} supply voltage

V_{CC} provides the power supply for all operations (Read, Program and Erase). The command interface is disabled when the V_{CC} supply voltage is less than the Lockout voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power-up, power-down and power surges. If the Program/Erase controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1 µF capacitor should be connected between the V_{CC} supply voltage pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations (see I_{CC1}, I_{CC2}, I_{CC3} in *Table 22: DC characteristics*).

2.13 V_{CCQ} input/output supply voltage

V_{CCQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.

2.14 V_{SS} ground

V_{SS} is the reference for all voltage measurements. The device features two V_{SS} pins; both of which must be connected to the system ground.

3 Bus Operations

There are five standard bus operations that control the device. These are Bus Read (Random and Page modes), Bus Write, Output Disable, Standby and Automatic Standby.

See *Table 3: Bus operations, 8-bit mode* and *Table 4: Bus operations, 16-bit mode* for a summary. Typical glitches of less than 5ns on Chip Enable, Write Enable, and Reset pins are ignored by the memory and do not affect bus operations.

3.1 Bus Read

Bus Read operations read from the memory cells, or specific registers in the command interface. To speed up the read operation the memory array can be read in Page mode where data is internally read and stored in a page buffer. The page has a size of 16 words (or 32bytes) and is addressed by the address inputs A3-A0 in x16 bus mode and A3-A0 plus DQ15/A–1 in x8 bus mode.The page read mode is not supported for reading Extended Memory Blocks and CFI information.

A valid Bus Read operation involves setting the desired address on the Address inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data inputs/outputs will output the value, see *Figure 16: Random Read AC waveforms (8-bit mode)*, *Figure 19: Page Read AC waveforms (16-bit mode)*, and *Table 23: Read AC characteristics*, for details of when the output becomes valid.

3.2 Bus Write

Bus Write operations write to the command interface. A valid Bus Write operation begins by setting the desired address on the Address inputs. The Address inputs are latched by the command interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data inputs/outputs are latched by the command interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See *Figure 20*, and *Figure 21*, Write AC waveforms, and *Table 24* and *Table 25*, Write AC characteristics, for details of the timing requirements.

3.3 Output Disable

The Data inputs/outputs are in the high impedance state when Output Enable is High, V_{IH}.

3.4 Standby

Driving Chip Enable High in Read mode, causes the memory to enter Standby mode and the data inputs/outputs pins are placed in the high-impedance state. To reduce the Supply current to the Standby Supply current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.3$ V. For the Standby current level see *Table 22: DC characteristics*.

During program or erase operations the memory will continue to use the Program/Erase Supply current, I_{CC3}, for Program or Erase operations until the operation completes.

3.5 Reset

During Reset mode the memory is deselected and the outputs are high impedance. The memory is in Reset mode when RST# is at V_{IL}. The power consumption is reduced to the standby level, independently from the Chip Enable, Output Enable or Write Enable inputs.

3.6 Auto Select mode

The Auto Select mode allows the system or the programming equipment to read the electronic signature, verify the protection status of the Extended Memory Block, and apply/remove Block protection. For example, this mode can be used by programming equipment to automatically match a device and the application code to be programmed.

At power-up, the device is in Read mode, and can then be put in Auto Select mode by issuing the Auto Select command (see *Section 6.1.2*).

The device cannot enter Auto Select mode when a program or erase operation is in progress (RY/BY# Low). However, Auto Select mode can be entered if the program or erase operation has been suspended by issuing a Program Suspend or Erase Suspend command (see *Section 6.1.6*).

The Auto Select mode is exited by performing a reset. The device is returned to Read mode, except if the Auto Select mode was entered after an Erase Suspend or a Program Suspend command. In this case, it returns to the Erase or Program Suspend mode.

3.6.1 Read electronic signature

The memory has two codes, the manufacturer code and the device code used to identify the memory. These codes can be accessed by performing read operations with control signals and addresses set as shown in *Table 5: Read electronic signature - auto select mode - programmer method (8-bit mode)* and *Table 6: Read electronic signature - auto select mode - programmer method (16-bit mode)*.

These codes can also be accessed by issuing an Auto Select command (see *Section 6.1.2: Auto Select command*).

3.6.2 Verify Extended Memory Block protection indicator

The Extended Memory Block is either Numonyx pre-locked or customer-lockable.

The protection status of the Extended Memory Block (pre-locked or customer-lockable) can be accessed by reading the Extended Memory Block protection indicator. It can be read in Auto Select mode using either the programmer (see *Table 7* and *Table 8*) or the in-system method (see *Table 9* and *Table 10*).

The protection status of the Extended Memory Block is then output on bit DQ7 of the Data input/outputs (see *Table 3* and *Table 4*, Bus operations in 8-bit and 16-bit mode).

3.6.3 Verify block protection status

The protection status of a block can be determined by performing a read operation with control signals and addresses set as shown in *Table 7* and *Table 8*.

If the block is protected, then 01h (in x 8 mode) is output on Data input/outputs DQ0-DQ7, otherwise 00h is output.

3.6.4 Hardware Block Protect

The V_{PP}/WP# pin can be used to protect the highest or lowest block. When V_{PP}/WP# is at V_{IL}, the highest block (M29EWH) or the lowest block (M29EWL) is protected and the other blocks remain with their own protection status.

Table 3. Bus operations, 8-bit mode

Operation[1]	CE#	OE#	WE#	RST#	V_{PP}/WP#	Address Inputs	Data Inputs/Outputs	
						Amax-A0, DQ15/A-1	DQ14-DQ8	DQ7-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Hi-Z	Data output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}[2]	Command address	Hi-Z	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z	Hi-Z

1. X = V_{IL} or V_{IH}.
2. If WP# is Low, V_{IL}, the outermost block remains protected.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 4. Bus operations, 16-bit mode

Operation[1]	CE#	OE#	WE#	RST#	V_{PP}/WP#	Address Inputs	Data Inputs/Outputs
						Amax-A0	DQ15/A-1, DQ14-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Data output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}[2]	Command address	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	V_{IH}	X	Hi-Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z

1. X = V_{IL} or V_{IH}.
2. If WP# is Low, V_{IL}, the outermost block remains protected.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 5. Read electronic signature - auto select mode - programmer method (8-bit mode)

Read cycle(1)	CE#	OE#	WE#	Address inputs								Data inputs/outputs	
				Amax-A7	A6	A5-A4	A3	A2	A1	A0	DQ15/A-1	DQ14-DQ8	DQ7-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	89h
Device code (cycle 1)							V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	7Eh
Device code (cycle 2)							V_{IH}	V_{IH}	V_{IH}	V_{IL}	X	X	22h (256-Mbit) 23h (512-Mbit) 28h (1-Gbit) 48h (2-Gbit)
Device code (cycle 3)							V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	01h

1. X = V_{IL} or V_{IH}.

Table 6. Read electronic signature - auto select mode - programmer method (16-bit mode)

Read cycle(1)	CE#	OE#	WE#	Address inputs							Data inputs/outputs
				Amax-A7	A6	A5-A4	A3	A2	A1	A0	DQ15/A-1, DQ14-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	0089h
Device code (cycle 1)							V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Device code (cycle 2)							V_{IH}	V_{IH}	V_{IH}	V_{IL}	2222h (256-Mbit) 2223h (512-Mbit) 2228h (1-Gbit) 2248h (2-Gbit)
Device code (cycle 3)							V_{IH}	V_{IH}	V_{IH}	V_{IH}	2201h

1. X = V_{IL} or V_{IH}.

Table 7. Block protection - auto select mode - programmer method (8-bit mode)

Operation[1]		CE#	OE#	WE#	Address inputs								Data inputs/outputs	
					Amax-A15	A14-A7	A6	A5-A4	A3-A2	A1	A0	DQ15/A-1	DQ14-DQ8	DQ7-DQ0
Verify Extended Memory Block protection indicator (bit DQ7)	M29EWL	V_{IL}	V_{IL}	V_{IH}	X	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	X	X	89h (Numonyx pre-locked) 09h (customer-lockable)
	M29EWH													99h (Numonyx pre-locked) 19h (customer-lockable)
Verify block protection status					BAd						V_{IL}			01h (protected) 00h (unprotected)

1. X = V_{IL} or V_{IH}. BAd = any address in the block.

Table 8. Block protection - auto select mode - programmer method (16-bit mode)

Operation[1]		CE#	OE#	WE#	Address inputs							Data inputs/outputs
					Amax-A15	A14-A7	A6	A5-A4	A3-A2	A1	A0	DQ15/A-1, DQ14-DQ0
Verify Extended Memory Block indicator (bit DQ7)	M29EWL	V_{IL}	V_{IL}	V_{IH}	X	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	0089h (Numonyx pre-locked) 0009h (customer-lockable)
	M29EWH											0099h (Numonyx pre-locked) 0019h (customer-lockable)
Verify block protection status					BAd						V_{IL}	0001h (protected) 0000h (unprotected)

1. X = V_{IL} or V_{IH}. BAd = any address in the block.

4 Hardware Protection

The M29EW features a V_{PP}/WP# pin that protects the highest or lowest block. Refer to *Section 2: Signal Descriptions* for a detailed description of the signal.

5 Software Protection

The M29EW has four different software protection modes:

- Volatile Protection
- Non-Volatile Protection
- Password Protection
- Password Access

On first use all parts default to operate in non-volatile Protection mode and the customer is free to activate the non-volatile or the password protection mode.

The desired protection mode is activated by setting either the one-time programmable Non-Volatile Protection Mode Lock bit, or the Password Protection Mode Lock bit of the Lock Register (see *Section 7.1: Lock Register*). Programming the Non-Volatile Protection Mode Lock bit or the Password Protection Mode Lock bit, to '0' will permanently activate the Non-volatile or the Password Protection mode, respectively. These two bits are one-time programmable and non-volatile: once the protection mode has been programmed, it cannot be changed and the device will permanently operate in the selected protection mode. It is recommended to activate the desired software protection mode when first programming the device.

The Non-volatile and Password Protection modes both provide non-volatile Protection. Volatilely protected blocks and non-volatilely protected blocks can co-exist within the memory array. However, the volatile Protection only control the protection scheme for blocks that are not protected using the non-volatile or password protection.

If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The device is shipped with all blocks unprotected. The block protection status can be read either by performing a read electronic signature (see *Table 5* and *Table 6*) or by issuing an Auto Select command (see *Table 16: Block Protection Status*).

For the lowest and highest blocks, an even higher level of block protection can be achieved by locking the blocks using the non-volatile Protection and then by holding the V_{PP}/WP# pin Low.

Password Access is a security enhancement offered on the M29EW device. This feature protects information stored in the main-array blocks by preventing content alteration or reads until a valid 64-bit password is received. Password Access may be combined with Non-Volatile and/or Volatile Protection to create a multi-tiered solution.

Please contact your Numonyx Sales for further details concerning Password Access feature.

5.1 Volatile Protection mode

The volatile Protection allows the software application to easily protect blocks against inadvertent change. However, the protection can be easily disabled when changes are needed. Volatile Protection bits, VPBs, are volatile and unique for each block and can be individually modified. VPBs only control the protection scheme for unprotected blocks that have their non-volatile Protection bits, NVPBs, cleared (erased to ‘1’) (see *Section 5.2: Non-Volatile Protection mode* and *Section 6.3.5: Non-Volatile Protection mode command set*).

By issuing the VPB Program or VPB Clear commands, the VPBs are set (programmed to ‘0’) or cleared (erased to ‘1’), thus placing associated blocks in the protected or unprotected state respectively. The VPBs can be set (programmed to ‘0’) or cleared (erased to ‘1’) as often as needed.

When the parts are first shipped, or after a power-up or hardware reset, the VPBs default to be cleared.

Refer to *Section 6.3.7* for a description of the volatile Protection mode command set.

5.2 Non-Volatile Protection mode

5.2.1 Non-Volatile Protection bits

A non-volatile Protection bit (NVPB) is assigned to each block.

When a NVPB is set to ‘0’, the associated block is protected, preventing any program or erase operations in this block.

The NVPB bits can be set individually by issuing a NVPB Program command. They are non-volatile and will remain set through a hardware reset or a power-down/power-up sequence.

The NVPBs cannot be cleared individually, they can only be all cleared at the same time by issuing a Clear all Non-Volatile Protection bits command.

The NVPBs can be protected all at a time by setting a volatile bit, the NVPB Lock bit (see *Section 5.2.2: Non-Volatile Protection Bit Lock bit*).

If one of the non-volatile protected blocks needs to be unprotected (corresponding NVPB set to ‘1’), a few more steps are required:

1. First, the NVPB Lock bit must be ‘1’ by either putting the device through a power cycle, or hardware reset.
2. The NVPBs can then be changed to reflect the desired settings.
3. The NVPB Lock bit must be set to ‘0’ once again to lock the NVPBs by associated command. The device operates normally again.

Note: 1 To achieve the best protection, it is recommended to execute the NVPB Lock Bit Program command early in the boot code and to protect the boot code by holding V_{PP}/WP# Low, V_{IL}.

2 The NVPBs and VPBs have the same function when V_{PP}/WP# pin is High, V_{IH}, as they do when V_{PP} /WP# pin is at the voltage for program acceleration (V_{PPH}).

Refer to *Table 16: Block Protection Status* and *Figure 5: Software protection scheme* for details on the block protection mechanism, and to *Section 6.3.5* for a description of the Non-Volatile Protection mode command set.

5.2.2 Non-Volatile Protection Bit Lock bit

The Non-Volatile Protection Bit Lock bit (NVPB Lock bit) is a global volatile bit for all NVPBs.

When set (programmed to ‘0’), it prevents changing the state of the NVPBs. When reset to ‘1’, the NVPBs can be set and reset using the NVPB Program command and Clear all NVPBs command, respectively.

There is only one NVPB Lock bit per device.

Refer to *Section 6.3.6* for a description of the NVPB Lock bit command set.

Note: 1 No software command unlocks this bit unless the device is in password protection mode; in standard non-volatile Protection mode, it can be cleared only by taking the device through a hardware reset or a power-up.

2 The NVPB Lock bit must be set (programmed to ‘0’) only after all NVPBs are configured to the desired settings.

5.3 Password Protection mode

The password protection mode provides an even higher level of security than the Non-Volatile Protection mode by requiring a 64-bit password for unlocking the device NVPB Lock bit.

In addition to this password requirement, the NVPB Lock bit is set ‘0’ after power-up and reset to maintain the device in password protection mode. Successful execution of the Password Unlock command by entering the correct password clears the NVPB Lock bit, allowing for block NVPBs to be modified.

If the password provided is incorrect, the NVPB Lock bit remains locked and the state of the NVPBs cannot be modified.

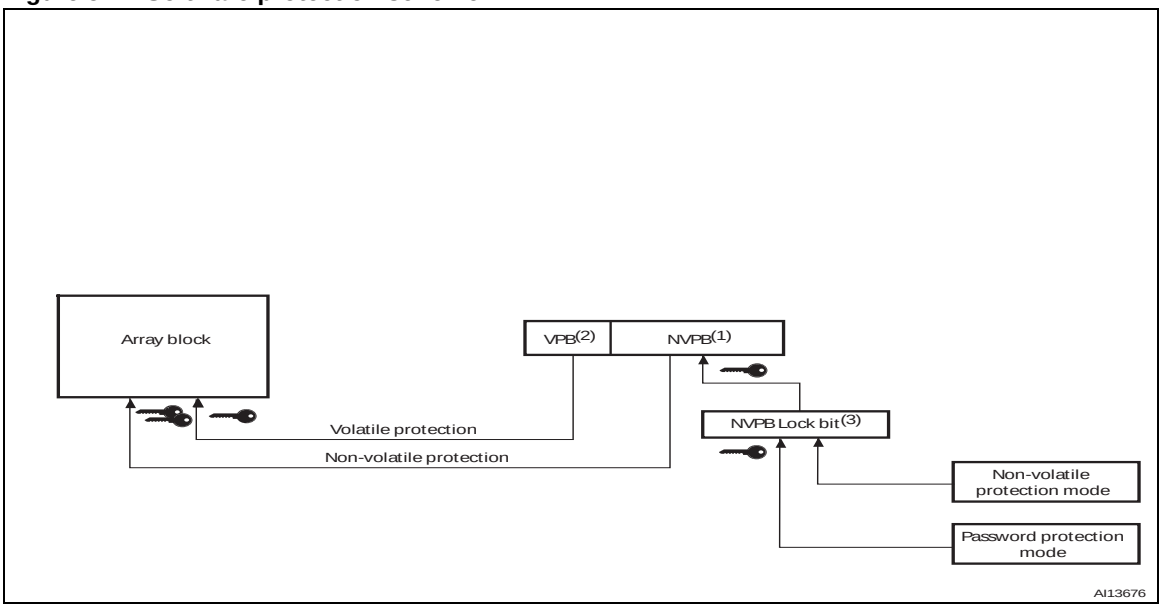
To place the device in password protection mode, the following steps are required:

1. Prior to activating the password protection mode, it is necessary to set a 64-bit password and to verify it (see *Password Program command* and *Password Read command*). Password verification is only allowed before the password protection mode is activated.
2. The password protection mode is then activated by programming the Password Protection Mode Lock bit to ‘0’. This operation is not reversible and once the bit is programmed it cannot be erased, the device permanently remains in password protection mode, and the 64-bit password can neither be retrieved nor reprogrammed. Moreover, all commands to the address where the password is stored, are disabled. Refer to *Table 16: Block Protection Status* and *Figure 5: Software protection scheme* for details on the block protection scheme.

Refer to *Section 6.3.4* for a description of the Password Protection mode command set.

Note: There is no means to verify the password after Password Protection mode is enabled. If the password is lost after enabling the Password Protection mode, there is no way to clear the NVPB Lock bit.

Figure 5. Software protection scheme



1. NVPBs default to ‘1’ (block unprotected) when shipped from Numonyx. A block is protected or unprotected when its NVPB is set to ‘0’ and ‘1’, respectively. NVPBs are programmed individually and cleared collectively.
2. VPB default status depends on ordering option. A block is protected or unprotected when its VPB is set to ‘0’ and ‘1’, respectively. VPBs can be programmed and cleared individually.
3. The NVPB Lock bit is volatile and default to ‘1’ (NVPB bits unlocked) after power-up or hardware reset. NVPB bits are locked by setting the NVPB Lock bit to ‘0’. Once programmed to ‘0’, the NVPB Lock bit can only be reset to ‘1’ by taking the device through a power-up or hardware reset.

6 Command Interface

All Bus Write operations to the memory are interpreted by the command interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes depending on whether the memory is in 16-bit or 8-bit mode.

Note: For 2-Gbit (1-Gbit/1-Gbit) device, all the set-up command should be re-issued to the device when different die is selected.

6.1 Standard commands

See either *Table 9*, or *Table 10*, depending on the configuration that is being used, for a summary of the standard commands.

6.1.1 Read/Reset command

The device enters read mode of main array memory after a reset or power-up sequence.

The Read/Reset command returns the memory to Read mode. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to Read mode. If the Read/Reset command is issued during the time-out of a Block erase operation, the memory will take up to 10 µs to abort. During the abort period no valid data can be read from the memory.

The Read/Reset command will not abort an Erase operation when issued while in Erase Suspend.

6.1.2 Auto Select command

The Auto Select command puts the device in Auto Select mode, once in Auto Select mode, the system can read the manufacturer code, the device code, the protection status of each block (Block Protection status) and the Extended Memory Block protection indicator.

Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued Bus Read operations to specific addresses output the manufacturer code, the device code, the Extended Memory Block protection indicator and a block protection status (see *Table 9* and *Table 10* in conjunction with *Table 5*, *Table 6*, *Table 7*, and *Table 8*). The memory remains in Auto Select mode until a Read/Reset or CFI Query command is issued.

6.1.3 Read CFI Query command

The memory contains an information area, named CFI data structure, which contains a description of various electrical and timing parameters, density information and functions supported by the memory. See *Appendix B*, *Table 34*, *Table 35*, *Table 36, Table 37* and *Table 38* for details on the information contained in the Common Flash Interface (CFI) memory area.

The Read CFI Query command is used to put the memory in Read CFI Query mode. Once in Read CFI Query mode, Bus Read operations to the memory will output data from the Common Flash Interface (CFI) memory area. One Bus Write cycle is required to issue the Read CFI Query command. This command is valid only when the device is in the Read Array or Auto Select mode.

The Read/Reset command must be issued to return the device to the previous mode (the Read Array mode or Auto Select mode). A second Read/Reset command is required to put the device in Read Array mode from Auto Select mode.

6.1.4 Chip Erase command

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase command and start the Program/Erase controller.

If some block are protected, then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100 µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Erase operation the memory will ignore all commands, including the Erase Suspend command. It is not possible to issue any command to abort the operation. Typical Chip Erase times are given in *Table 28*. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data inputs/outputs. See *Section 7.2: Status Register* for more details.

After the Chip Erase operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Chip Erase command sets all of the bits in unprotected blocks of the memory to ‘1’. All previous data is lost.

The Chip Erase operation is aborted by performing a reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended to erase again the entire chip.

6.1.5 Block Erase command

The Block Erase command can be used to erase a list of one or more blocks. It sets all of the bits in the unprotected selected blocks to ‘1’. All previous data in the selected blocks is lost.

Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. After the command sequence is written, a Block Erase time-out occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Once the Program/Erase controller has started, it is not possible to select

any more blocks. Each additional block must therefore be selected within the time-out period of the last block. The time-out timer restarts when an additional block is selected. After the sixth Bus Write operation, a Bus Read operation outputs the Status Register. See *Figure 20: Write Enable Controlled Program waveforms (8-bit mode)* and *Figure 21: Write Enable Controlled Program waveforms (16-bit mode)* for details on how to identify if the Program/Erase controller has started the Block Erase operation.

After the Block Erase operation has completed, the memory returns to the Read mode, unless an error has occurred. When an error occurs, Bus Read operations will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100 µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory ignores all commands except the Erase Suspend command and the Read/Reset command which is only accepted during the time-out period. Typical Block Erase time and Block Erase time-out are given in *Table 28: Programming and Erase Performance*.

The Block Erase operation is aborted by performing a reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended to erase again the blocks aborted.

6.1.6 Erase Suspend command

The Erase Suspend command can be used to temporarily suspend a Block Erase operation. One Bus Write operation is required to issue the command together with the block address.

After the command sequence is written, a minimum Block Erase time-out occurs (see *Section 6.1.6: Erase Suspend command*). During the time-out period, additional block addresses and block erase commands can be written.

The Program/Erase controller suspends the erase operation within the Erase Suspend Latency time of the Erase Suspend command being issued. However, when the Erase Suspend command is written during the Block Erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

Once the Program/Erase controller has stopped, the memory operates in Read mode and the Erase is suspended.

During Erase Suspend it is possible to read and execute Program or Write to Buffer Program operations in blocks that are not suspended; both read and program operations behave as normal on these blocks. Reading from blocks that are suspended will output the Status Register. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. In this case the Status Register is not read and no error condition is given.

It is also possible to issue the Auto Select, Read CFI Query and Unlock Bypass commands during an Erase Suspend. The Read/Reset command must be issued to return the device to Read Array mode before the Resume command will be accepted.

During Erase Suspend a Bus Read operation to the Extended Memory Block will output the Extended Memory Block data. Once in the Extended Memory Block mode, the Exit

Extended Memory Block command must be issued before the erase operation can be resumed.

The Erase Suspend command is ignored if written during Chip Erase operations.

Refer to *Table 28: Programming and Erase Performance* for the values of Block Erase time-out and Block Erase Suspend latency time.

If the Erase Suspend operation is aborted by performing a reset or powering down the device, data integrity cannot be ensured, and it is recommended to erase again the blocks suspended.

6.1.7 Erase Resume command

The Erase Resume command is used to restart the Program/Erase controller after an Erase Suspend.

The device must be in Read Array mode before the Resume command will be accepted. An erase can be suspended and resumed more than once.

6.1.8 Program Suspend command

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any block. When the Program Suspend command is issued during a program operation, the device suspends the program operation within the Program Suspend latency time (see *Table 28: Programming and Erase Performance*) and updates the Status Register bits.

After the program operation has been suspended, the system can read array data from any address. However, data read from program-suspended addresses is not valid.

The Program Suspend command may also be issued during a program operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Extended Memory Block area (one-time program area), the user must use the proper command sequences to enter and exit this region.

The system may also issue the Auto Select command sequence when the device is in the Program Suspend mode. The system can read as many Auto Select codes as required. When the device exits the Auto Select mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Auto Select command sequence for more information.

If the Program Suspend operation is aborted by performing a reset or powering down the device, data integrity cannot be ensured, and it is recommended to program again the words or bytes aborted.

6.1.9 Program Resume command

After the Program Resume command is issued, the device reverts to programming. The controller can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to *Figure 20: Write Enable Controlled Program waveforms (8-bit mode)* and *Figure 21: Write Enable Controlled Program waveforms (16-bit mode)* for details.

The system must issue a Program Resume command, to exit the Program Suspend mode and to continue the programming operation.

Further issuing of the Resume command is ignored. Another Program Suspend command can be written after the device has resumed programming.

6.1.10 Program command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase controller.

Programming can be suspended and then resumed by issuing a Program Suspend command and a Program Resume command, respectively (see *Section 6.1.8: Program Suspend command* and *Section 6.1.9: Program Resume command*).

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

After programming has started, Bus Read operations output the Status Register content. See *Figure 20: Write Enable Controlled Program waveforms (8-bit mode)* and *Figure 21: Write Enable Controlled Program waveforms (16-bit mode)* for more details. Typical program times are given in *Table 28: Programming and Erase Performance*.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs, Bus Read operations to the memory continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

One of the Erase commands must be used to set all the bits in a block or in the whole memory from ‘0’ to ‘1’.

The Program operation is aborted by performing a reset or powering-down the device. In this case data integrity cannot be ensured, and it is recommended to reprogram the word or byte aborted.

Table 9. Standard commands, 8-bit mode

Command		Length	Bus operations[1]											
			1st		2nd		3rd		4th		5th		6th	
			Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset		1	X	F0	-	-	-	-	-	-	-	-	-	-
		3	AAA	AA	555	55	X	F0	-	-	-	-	-	-
Auto Select	Manufacturer code	3	AAA	AA	555	55	AAA	90	(2)(3)	(2)(3)	-	-	-	-
	Device code													
	Extended Memory Block protection indicator													
	Block protection status													
Program[4]		4	AAA	AA	555	55	AAA	A0	PA	PD	-	-	-	-
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Block Erase		6+	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30
Erase/Program Suspend		1	X	B0	-	-	-	-	-	-	-	-	-	-
Erase/Program Resume		1	X	30	-	-	-	-	-	-	-	-	-	-
Read CFI Query		1	AA	98	-	-	-	-	-	-	-	-	-	-

1. X = Don't care, PA = Program Address, PD = Program Data, BAd = Any address in the Block. All values in the table are in hexadecimal.
2. These cells represent Read cycles. The other cells are Write cycles.
3. The Auto Select addresses and data are given in *Table 5: Read electronic signature - auto select mode - programmer method (8-bit mode)*, and *Table 7: Block protection - auto select mode - programmer method (8-bit mode)*, except for A9 that is 'Don't care'.
4. In Unlock Bypass, the first two unlock cycles are no more needed (see *Table 11: Fast Program commands, 8-bit mode* and *Table 12: Fast Program commands, 16-bit mode*).

Table 10. Standard commands, 16-bit mode

Command		Length	Bus operations[1]											
			1st		2nd		3rd		4th		5th		6th	
			Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset		1	X	F0	-	-	-	-	-	-	-	-	-	-
		3	555	AA	2AA	55	X	F0	-	-	-	-	-	-
Auto Select	Manufacturer code	3	555	AA	2AA	55	555	90	(2)(3)	(2)(3)	-	-	-	-
	Device code													
	Extended Memory Block protection indicator													
	Block protection status													
Program[4]		4	555	AA	2AA	55	555	A0	PA	PD	-	-	-	-
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase		6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BAd	30
Erase/Program Suspend		1	X	B0	-	-	-	-	-	-	-	-	-	-
Erase/Program Resume		1	X	30	-	-	-	-	-	-	-	-	-	-
Read CFI Query		1	55	98	-	-	-	-	-	-	-	-	-	-

1. X = Don't care, PA = Program Address, PD = Program Data, BAd = any address in the Block. All values in the table are in hexadecimal.
2. These cells represent Read cycles. The other cells are Write cycles.
3. The Auto Select addresses and data are given in *Table 6: Read electronic signature - auto select mode - programmer method (16-bit mode)*, and *Table 8: Block protection - auto select mode - programmer method (16-bit mode)*, except for A9 that is 'Don't care'.
4. In Unlock Bypass, the first two unlock cycles are no more needed (see *Table 11* and *Table 12* Fast Program commands**,** 8-bit and 16-bit mode).

6.2 Fast Program commands

The M29EW offers a set of Fast Program commands to improve the programming throughput:

- Write to Buffer Program
- Unlock Bypass

See either *Table 11: Fast Program commands, 8-bit mode on page 39* or *Table 12: Fast Program commands, 16-bit mode on page 39* depending on the configuration that is being used, for a summary of the Fast Program commands.

When V_{PPH} is applied to the V_{PP}/Write Protect pin the memory automatically enters Unlock Bypass mode (see *Section 6.2.4: Unlock Bypass command*).

After programming has started, Bus Read operations in the memory output the Status Register content. Write to Buffer Program command can be suspended and then resumed by issuing a Program Suspend command and a Program Resume command, respectively (see *Section 6.1.8: Program Suspend command* and *Section 6.1.9: Program Resume command*).

After the fast program operation has completed, the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read operations to the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ‘0’ to ‘1’.

Typical program times are given in *Table 28: Programming and Erase Performance*.

6.2.1 Write to Buffer Program command

The Write to Buffer Program command makes use of the device’s 512-word program buffer to speed up programming. A maximum of 512 words can be loaded into the program buffer. The Write to Buffer Program command dramatically reduces system programming time compared to the standard non-buffered Program command.

When issuing a Write to Buffer Program command, the V_{PP}/WP# pin can be either held High, V_{IH}, or raised to V_{PPH}.

See *Table 28* for details on typical Write to Buffer Program times in both cases.

Five successive steps are required to issue the Write to Buffer Program command:

1. The Write to Buffer Program command starts with two unlock cycles.
2. The third Bus Write cycle sets up the Write to Buffer Program command. The set-up code can be addressed to any location within the targeted block.
3. The fourth Bus Write cycle sets up the number of words/bytes to be programmed. Value N is written to the same block address, where N+1 is the number of words/bytes to be programmed. N+1 must not exceed the size of the program buffer or the operation will abort.
4. The fifth cycle loads the first address and data to be programmed.
5. Use N Bus Write cycles to load the address and data for each word/byte into the program buffer. Addresses must lie within the range from the start address+1 to the start address + N-1. Optimum programming performance and lower power usage are obtained by aligning the starting address at the beginning of a 512-word boundary (A[8:0] = 0x000h). Any buffer size smaller than 512-word is allowed within 512-word boundary, while All the addresses used in the Write to Buffer Program operation must

lie within the 512-word boundary. In addition, any crossing boundary buffer program will result in a program abort. See *Figure 6* for details of the available program buffer size.

To program the content of the program buffer, this command must be followed by a Write to Buffer Program Confirm command.

If an address is written several times during a Write to Buffer Program operation, the address/data counter will be decremented at each data load operation and the data will be programmed to the last word loaded into the buffer.

Invalid address combinations or failing to follow the correct sequence of Bus Write cycles will abort the Write to Buffer Program.

The Status Register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during a Write to Buffer Program operation.

It is possible to detect Program operation fails when changing programmed data from ‘0’ to ‘1’, that is when reprogramming data in a portion of memory already programmed. The resulting data will be the logical OR between the previous value and the current value.

See *Figure 7: Write to Buffer Program fletcher and pseudo code*, for a suggested flow chart on using the Write to Buffer Program command.

Figure 6. Boundary condition of program buffer size

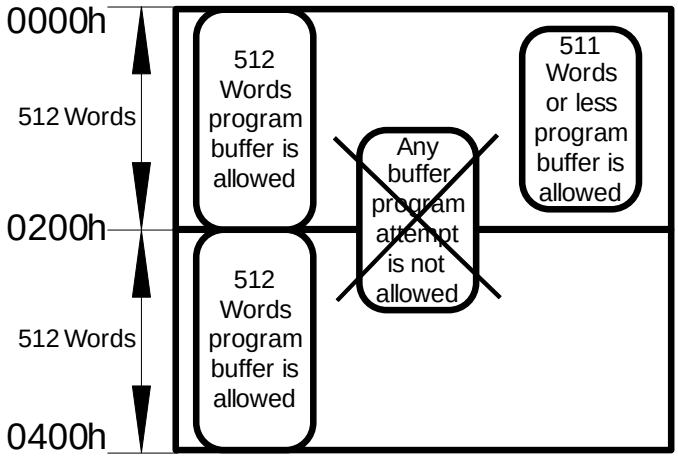
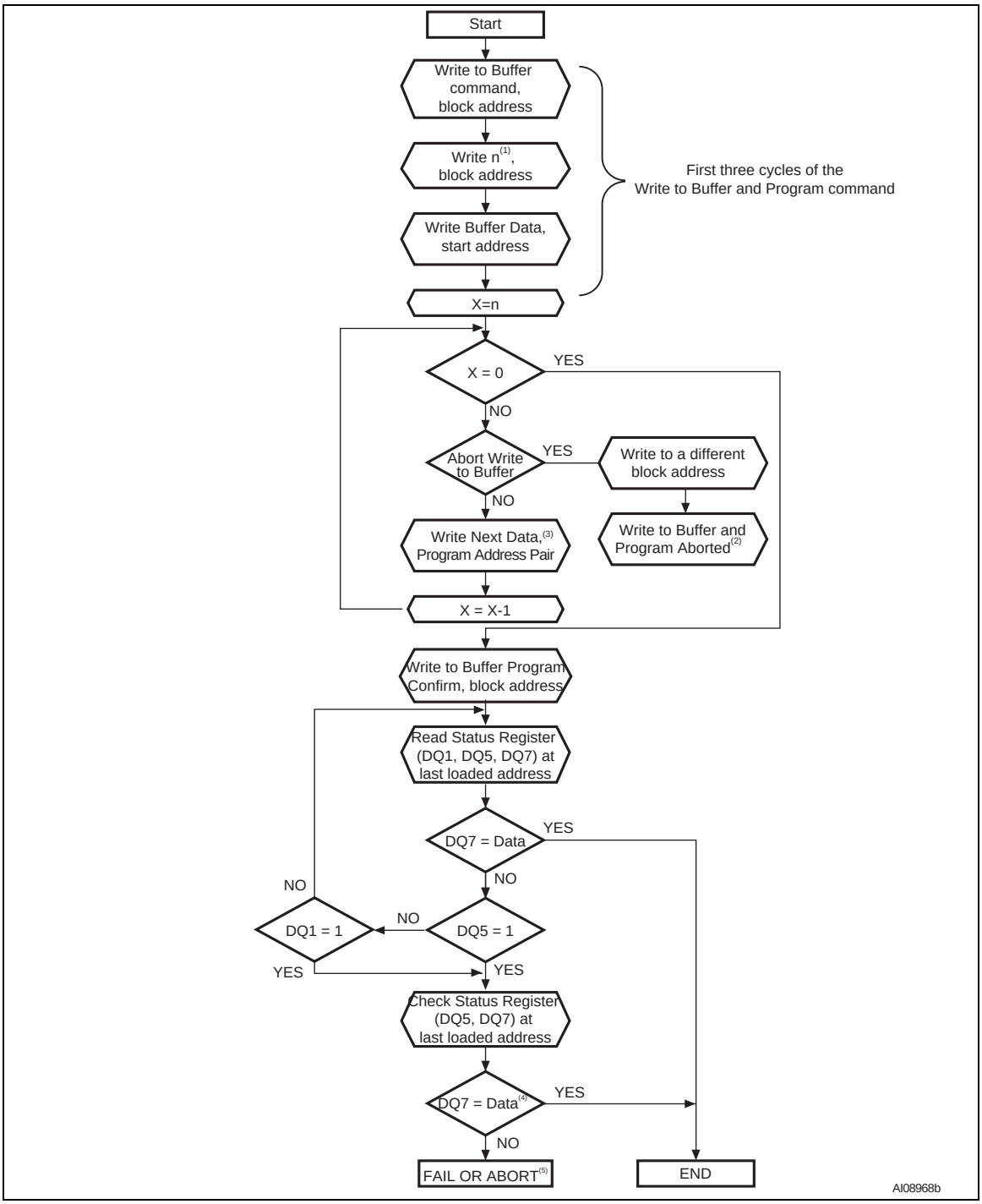


Figure 7. Write to Buffer Program fletcher and pseudo code



1. n+1 is the number of addresses to be programmed.
2. A Write to Buffer Program Abort and Reset must be issued to return the device in Read mode.
3. When the block address is specified, any address in the selected block address space is acceptable. However when

loading program buffer address with data, all addresses must fall within the selected program buffer page.

4. DQ7 must be checked since DQ5 and DQ7 may change simultaneously.
5. If this flow chart location is reached because DQ5='1', then the Write to Buffer Program command failed. If this flow chart location is reached because DQ1='1', then the Write to Buffer Program command aborted. In both cases, the appropriate reset command must be issued to return the device in Read mode: a Reset command if the operation failed, a Write to Buffer Program Abort and Reset command if the operation aborted.
6. See *Table 9* and *Table 10*, for details on Write to Buffer Program command sequence.

6.2.2 Buffered Program Abort and Reset command

A Buffered Program Abort and Reset command must be issued to abort the Buffer Program operation and reset the device in Read mode.

The buffer programming sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the number of locations to program step in the Write to Buffer Program command.
- Write to an address in a block different than the one specified during the write-buffer-load command.
- Write an address/data pair to a different write-buffer-page than the one selected by the starting address during the program buffer data loading stage of the operation.
- Write data other than the Confirm command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = $\overline{DQ7}$ (for the last address location loaded), DQ6 = toggle, and DQ5 = 0 (all of which are Status Register bits). A Buffered Program Abort and Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Buffered Program Abort and Reset command sequence is required when using Buffer Programming features in Unlock Bypass mode.

6.2.3 Write to Buffer Program Confirm command

The Write to Buffer Program Confirm command is used to confirm a Write to Buffer Program command and to program the N+1 words/bytes loaded in the program buffer by this command.

6.2.4 Unlock Bypass command

The Unlock Bypass command is used to place the device in Unlock Bypass mode. When the device enters the Unlock Bypass mode, the two initial unlock cycles required in the standard program command sequence are no more needed, and only two write cycles are required to program data, instead of the normal four cycles (see *Note 4* below *Table 9* and *Table 10*). This results in a faster total programming time.

Unlock Bypass command is consequently used in conjunction with the Unlock Bypass Program command to program the memory faster than with the standard program commands. When the cycle time to the device is long, considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

When in Unlock Bypass mode, only the Unlock Bypass Program, Unlock Bypass Block Erase, Unlock Bypass Chip Erase, and Unlock Bypass Reset commands are valid:

- The Unlock Bypass Program command can be issued to program addresses within the memory.
- The Unlock Bypass Block Erase command can then be issued to erase one or more memory blocks.
- The Unlock Bypass Chip Erase command can be issued to erase the whole memory array.
- The Unlock Bypass Write to Buffer Program command can be issued to speed up programming operation.
- The Unlock Bypass Reset command can be issued to return the memory to Read mode.

In Unlock Bypass mode the memory can be read as if in Read mode.

6.2.5 Unlock Bypass Program command

The Unlock Bypass Program command can be used to program one address in the memory array at a time. The command requires two Bus Write operations, the final write operation latches the address and data and starts the Program/Erase controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. The operation cannot be aborted, a Bus Read operation to the memory outputs the Status Register. See the program command in *Table 11.: Fast Program commands, 8-bit mode* and *Table 12.: Fast Program commands, 16-bit mode* for more details.

6.2.6 Unlock Bypass Block Erase command

The Unlock Bypass Block Erase command can be used to Erase one or more memory blocks at a time. The command requires two Bus Write operations instead of six using the standard Block Erase command. The final Bus Write operation latches the address of the block and starts the Program/Erase controller.

To erase multiple block (after the first two Bus Write operations have selected the first block in the list), each additional block in the list can be selected by repeating the second Bus Write operation using the address of the additional block.

The Unlock Bypass Block Erase command behaves in the same way as the Block Erase command: the operation cannot be aborted, and a Bus Read operation to the memory outputs the Status Register (see *Section 6.1.5: Block Erase command* for details).

6.2.7 Unlock Bypass Chip Erase command

The Unlock Bypass Chip Erase command can be used to erase all memory blocks at a time. The command requires two Bus Write operations only instead of six using the standard Chip Erase command. The final Bus Write operation starts the Program/Erase controller.

The Unlock Bypass Chip Erase command behaves in the same way as the Chip Erase command: the operation cannot be aborted, and a Bus Read operation to the memory outputs the Status Register (see *Section 6.1.4: Chip Erase command* for details).

6.2.8 Unlock Bypass Write to Buffer Program command

The Unlock Bypass Write to Buffer command can be used to program the memory in Fast Program mode. The command requires two Bus Write operations less than the standard Write to Buffer Program command.

The Unlock Bypass Write to Buffer Program command behaves in the same way as the Write to Buffer Program command: the operation cannot be aborted and a Bus Read operation to the memory outputs the Status Register (see *Section 6.2.1: Write to Buffer Program command* for details).

The Write to Buffer Program Confirm command is used to confirm an Unlock Bypass Write to Buffer Program command and to program the N+1 words/bytes loaded in the program buffer by this command.

6.2.9 Unlock Bypass Reset command

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from Unlock Bypass mode.

Table 11. Fast Program commands, 8-bit mode

Command	Length	Bus Write operations(1)									
		1st		2nd		3rd		4th		5th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Write to Buffer Program	N+5	AAA	AA	555	55	BAd	25	BAd	N(2)	PA(3)	PD
Write to Buffer Program Confirm	1	BAd(4)	29	-	-	-	-	-	-	-	-
Buffered Program Abort and Reset	3	AAA	AA	555	55	AAA	F0	-	-	-	-
Unlock Bypass	3	AAA	AA	555	55	AAA	20	-	-	-	-
Unlock Bypass Program	2	X	A0	PA	PD	-	-	-	-	-	-
Unlock Bypass Block Erase	2+	X	80	BAd	30	-	-	-	-	-	-
Unlock Bypass Chip Erase	2	X	80	X	10	-	-	-	-	-	-
Unlock Bypass Write to Buffer Program	N+3	BAd	25	BAd	N(2)	PA(3)	PD	-	-	-	-
Unlock Bypass Reset	2	X	90	X	00	-	-	-	-	-	-

1. X = Don't care, PA = Program Address, PD = Program Data, BAd = Any address in the Block. All values in the table are in hexadecimal.
2. The maximum number of cycles in the buffer program command sequence is 261. The maximum number of cycles in the unlock bypass buffer program command sequence is 259. N+1 is the number of bytes to be programmed during the Write to Buffer Program operation.
3. Amax-A7 address pin should be consistently unchanged. A0-A6 and A-1 pins are used to select a byte within the N+1 byte page.
4. BAd must be identical to the address loaded during the Write to Buffer Program 3rd and 4th cycles.

Table 12. Fast Program commands, 16-bit mode

Command	Length	Bus Write operations(1)									
		1st		2nd		3rd		4th		5th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Write to Buffer Program	N+5	555	AA	2AA	55	BAd	25	BAd	N(2)	PA(3)	PD
Write to Buffer Program Confirm	1	BAd(4)	29	-	-	-	-	-	-	-	-
Buffered Program Abort and Reset	3	555	AA	2AA	55	555	F0	-	-	-	-
Unlock Bypass	3	555	AA	2AA	55	555	20	-	-	-	-

Table 12. Fast Program commands, 16-bit mode

Command	Length	Bus Write operations[1]									
		1st		2nd		3rd		4th		5th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Unlock Bypass Program	2	X	A0	PA	PD	-	-	-	-	-	-
Unlock Bypass Block Erase	2+	X	80	BAd	30	-	-	-	-	-	-
Unlock Bypass Chip Erase	2	X	80	X	10	-	-	-	-	-	-
Unlock Bypass Write to Buffer Program	N+3	BAd	25	BAd	N[2]	PA[3]	PD	-	-	-	-
Unlock Bypass Reset	2	X	90	X	00	-	-	-	-	-	-

1. X = Don't care, PA = Program Address, PD = Program Data, BAd = Any address in the Block. All values in the table are in hexadecimal.
2. The maximum number of cycles in the buffer program command sequence is 517. The maximum number of cycles in the unlock bypass buffer program command sequence is 515. N+1 is the number of bytes to be programmed during the Write to Buffer Program operation.
3. Amax-A9 address pins should be consistently unchanged. A0-A8 pins are used to select a word within the N+1 word page.
4. BAd must be identical to the address loaded during the Write to Buffer Program 3rd and 4th cycles.

6.3 Protection commands

Blocks can be protected individually against accidental program, erase or read operations. The device block protection scheme is shown in *Figure 5: Software protection scheme*. See either *Table 13*, or *Table 14*, depending on the configuration that is being used, for a summary of the Block Protection commands.

Block protection commands are available both in 8-bit and 16-bit configuration.

The protections of both memory blocks and Extended Memory Block protection are configured through the Lock register (see *Section 7.1: Lock Register*).

6.3.1 Enter Extended Memory Block command

The M29EW has one extra 128-word Extended Memory Block that can only be accessed using the Enter Extended Memory Block command.

Three Bus Write cycles are required to issue the Enter Extended Memory Block command. Once the command has been issued the device enters the Extended Memory Block mode where all Bus Read or Program operations are conducted on the Extended Memory Block. Once the device is in the Extended Memory Block mode, the Extended Memory Block is addressed by using the addresses occupied by block 0 in the other operating modes (see *Figure 4: Block addresses on page 11*).

The device remains in Extended Memory Block mode until the Exit Extended Memory Block command is issued or power is removed from the device. After a power-up sequence or hardware reset, the device will revert to reading from memory blocks in the main array.

The Extended Memory Block cannot be erased, and each bit of the Extended Memory Block can only be programmed once.

In Extended Memory Block mode, Erase, Chip Erase, Erase Suspend and Erase Resume commands are not allowed.

To exit from the Extended Memory Block mode the Exit Extended Memory Block command must be issued.

The Extended Memory Block is protected from further modification by programming Lock Register bit 0 (see *Section 7.1: Lock Register*). Once invoked, this protection cannot be undone.

6.3.2 Exit Extended Memory Block command

The Exit Extended Memory Block command is used to exit from the Extended Memory Block mode and return the device to Read mode. Four Bus Write operations are required to issue the command.

6.3.3 Lock Register command set

The M29EW offers a set of commands to access the Lock Register and to configure and verify its content. See the following sections in conjunction with *Section 7.1: Lock Register*, *Table 13* and *Table 14*.

Enter Lock Register Command Set command

Three Bus Write cycles are required to issue the Enter Lock Register Command Set command. Once the command has been issued, all Bus Read or Program operations are issued to the Lock Register.

Lock Register Program and Lock Register Read command

The Lock Register Program command allows to configure the Lock Register. The programmed data can then be checked by issuing a Lock Register Read command.

An Exit Protection Command Set command must then be issued to return the device to Read mode (see *Section 6.3.8: Exit Protection command set*).

6.3.4 Password Protection mode command set

Enter Password Protection Command Set command

Three Bus Write cycles are required to issue the Enter Password Protection Command Set command. Once the command has been issued, the commands related to the Password Protection mode can be issued to the device.

Password Program command

The Password Program command is used to program the 64-bit password used in the Password Protection mode.

To program the 64-bit password, the complete command sequence must be entered eight times at eight consecutive addresses selected by A1-A0 plus DQ15/A-1 in 8-bit mode, or four times at four consecutive addresses selected by A1-A0 in 16-bit mode.

The password can be checked by issuing a Password Read command.

Once Password Program operation has completed, an Exit Protection Command Set command must be issued to return the device to Read mode. The Password Protection mode can then be selected.

By default, all Password bits are set to ‘1’.

Note: In order to use password protection feature on 2-Gbit (1-Gbit/1-Gbit stack) device, the password must be programmed to both upper die and bottom die respectively.

Password Read command

The Password Read command is used to verify the Password used in Password Protection mode.

To verify the 64-bit password, the complete command sequence must be entered eight times at eight consecutive addresses selected by A1-A0 plus DQ15/A-1 in 8-bit mode, or four times at four consecutive addresses selected by A1-A0 in 16-bit mode.

If the Password Mode Lock bit is programmed and the user attempts to read the password, the device will output FFh onto the I/O data bus.

An Exit Protection Command Set command must be issued to return the device to Read mode.

Password Unlock command

The Password Unlock command is used to clear the NVPB Lock bit allowing to modify the NVPBs.

The Password Unlock command must be issued along with the correct password.

There must be a 1 µs delay between successive Password Unlock commands in order to prevent hackers from cracking the password by trying all possible 64-bit combinations. If this delay is not respected, the latest command will be ignored.

Approximately 1 µs is required for unlocking the device after the valid 64-bit password has been provided.

6.3.5 Non-Volatile Protection mode command set

Enter Non-Volatile Protection Command Set command

Three Bus Write cycles are required to issue the Enter Non-Volatile Protection Command Set command. Once the command has been issued, the commands related to the Non-Volatile Protection mode can be issued to the device.

Non-Volatile Protection Bit Program command (NVPB Program)

A block can be protected from program or erase by issuing a Non-Volatile Protection Bit command along with the block address. This command sets the NVPB to ‘1’ for a given block.

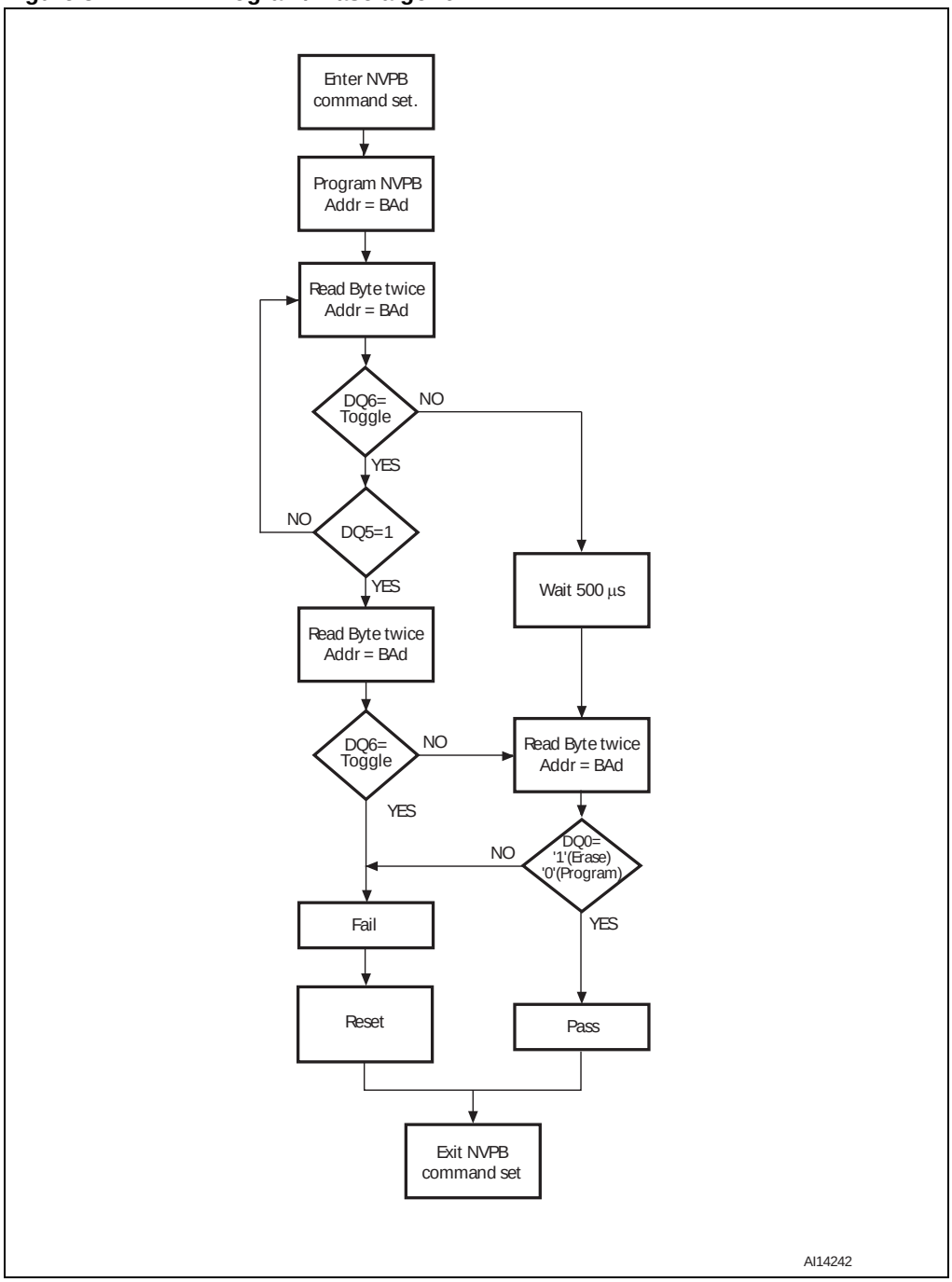
Read Non-Volatile Protection Bit Status command (Read NVPB Status)

The status of a NVPB for a given block or group of blocks can be read by issuing a Read Non-Volatile Modify Protection Bit command along with the block address.

Clear all Non-Volatile Protection Bits command (Clear all NVPBs)

The NVPBs are erased simultaneously by issuing a Clear all Non-Volatile Protection Bits command. No specific block address is required. If the NVPB Lock bit is set to ‘0’, the command fails.

Figure 8. NVPB Program/Erase algorithm



6.3.6 NVPB Lock Bit command set

Enter NVPB Lock Bit Command Set command

Three bus Write cycles are required to issue the Enter NVPB Lock Bit Command Set command. Once the command has been issued, the commands allowing to set the NVPB Lock bit can be issued to the device.

NVPB Lock Bit Program command

This command is used to set the NVPB Lock bit to ‘0’ thus locking the NVPBs, and preventing them from being modified.

Read NVPB Lock Bit Status command

This command is used to read the status of the NVPB Lock bit.

6.3.7 Volatile Protection mode command set

Enter Volatile Protection Command Set command

Three bus Write cycles are required to issue the Enter Volatile Protection Command Set command. Once the command has been issued, the commands related to the Volatile Protection mode can be issued to the device.

Volatile Protection Bit Program command (VPB Program)

The VPB Program command individually sets a VPB to ‘0’ for a given block.

If the NVPB for the same block is set, the block is locked regardless of the value of the VPB bit. (see *Table 16: Block Protection Status*).

Read VPB Status command

The status of a VPB for a given block can be read by issuing a Read VPB Status command along with the block address.

VPB Clear command

The VPB Clear command individually clears (sets to ‘1’) the VPB for a given block.

If the NVPB for the same block is set, the block is locked regardless of the value of the VPB bit. (see *Table 16: Block Protection Status*).

6.3.8 Exit Protection command set

The Exit Protection Command Set command is used to exit from the Lock Register, Password Protection, Non-Volatile Protection, Volatile Protection, and NVPB Lock Bit Command Set mode. It return the device to Read mode.

Table 13. Block Protection commands, 8-bit mode(1)(2)(3)

	Command	Length	Bus operations																					
			1st		2nd		3rd		4th		5th		6th		7th		8th		9th		10th		11th	
			Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data
Lock Register	Enter Lock Register Command Set(4)	3	AAA	AA	555	55	AAA	40	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Lock Register Program	2	X	A0	X	DATA(5)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Lock Register Read	1	X	DATA(5)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Password Protection	Enter Password Protection Command Set(4)	3	AAA	AA	555	55	AAA	60	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Password Program (6)(7)	2	X	A0	PWAn	PWDn	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Password Read	8	00	PWD0	01	PWD1	02	PWD2	03	PWD3	04	PWD4	05	PWD5	06	PWD6	07	PWD7	-	-	-	-	-	-
	Password Unlock(7)	11	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	04	PWD4	05	PWD5	06	PWD6	07	PWD7	00	29
Non-Volatile Protection	Enter Non-Volatile Protection Command Set(4)	3	AAA	AA	555	55	AAA	C0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	NVPB Program(8)	2	X	A0	BAd	00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Clear all NVPBs(9)	2	X	80	00	30	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Read NVPB Status (8)	1	BAd	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NVPB Lock bit	Enter NVPB Lock Bit Command Set	3	AAA	AA	555	55	AAA	50	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	NVPB Lock Bit Program(8)	2	X	A0	X	00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Read NVPB Lock Bit Status (8)	1	X	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Volatile Protection	Enter Volatile Protection Command Set	3	AAA	AA	555	55	AAA	E0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	VPB Program(8)	2	X	A0	BAd	00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Read VPB Status	1	BAd	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	VPB Clear(8)	2	X	A0	BAd	01	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Exit Protection Command Set (10)		2	X	90	X	00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Enter Extended Memory Block(4)		3	AAA	AA	555	55	AAA	88	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Exit Extended Memory Block		4	AAA	AA	555	55	AAA	90	X	00	-	-	-	-	-	-	-	-	-	-	-	-	-	-

1. Ad = address; Dat = data; BAd = Any address in the Block; RD = Read data; PWDn = Password byte 0 to 7; PWAn = Password Address (n = 0 to 7); X = Don't care. All values in the table are in hexadecimal.
2. Grey cells represent Read cycles. The other cells are Write cycles.
3. DQ15 to DQ8 are 'Don't care' during unlock and command cycles. Amax to A16 are 'Don't care' during unlock and command cycles unless an address is required.
4. An Enter command sequence must be issued prior to any operation. It disables read and write operations from and to block 0. Read and write operations from any other block are allowed.
5. DATA = Lock Register content.
6. Only one portion of password can be programmed or read by each Password Program command.
7. The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.
8. Protected and unprotected states correspond to 00 and 01, respectively.
9. The Clear all NVPBs command programs all NVPBs before erasure in order to prevent the over-erasure of previously cleared Non Volatile Modify Protection bits.
10. If an Entry Command Set command is issued, an Exit Protection Command Set command must be issued to return the device to Read mode.

Table 14. Block Protection commands, 16-bit mode(1)(2)(3)

	Command	Length	Bus operations													
			1st		2nd		3rd		4th		5th		6th		7th	
			Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data
Lock register	Enter Lock Register Command Set(4)	3	555	AA	2AA	55	555	40	-	-	-	-	-	-	-	-
	Lock Register Program	2	X	A0	X	DATA(5)	-	-	-	-	-	-	-	-	-	-
	Lock Register Read	1	X	DATA (5)	-	-	-	-	-	-	-	-	-	-	-	-
Password Protection	Enter Password Protection Command Set(4)	3	555	AA	2AA	55	555	60	-	-	-	-	-	-	-	-
	Password Program (6)(7)	2	X	A0	PWAn	PWDn	-	-	-	-	-	-	-	-	-	-
	Password Read	4	00	PWD0	01	PWD1	02	PWD2	03	PWD3	-	-	-	-	-	-
	Password Unlock(7)	7	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	00	29
Non-Volatile Protection	Enter Non-Volatile Protection Command Set(4)	3	555	AA	2AA	55	555	C0	-	-	-	-	-	-	-	-
	NVPB Program(8)	2	X	A0	BAd	00	-	-	-	-	-	-	-	-	-	-
	Clear all NVPBs(9)	2	X	80	00	30	-	-	-	-	-	-	-	-	-	-
	Read NVPB Status	1	BAd	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-
NVPB Lock bit	Enter NVPB Lock Bit Command Set	3	555	AA	2AA	55	555	50	-	-	-	-	-	-	-	-
	NVPB Lock Bit Program	2	X	A0	X	00	-	-	-	-	-	-	-	-	-	-
	Read NVPB Lock Bit Status	1	X	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-
Volatile Protection	Enter Volatile Protection Command Set	3	555	AA	2AA	55	555	E0	-	-	-	-	-	-	-	-
	VPB Program	2	X	A0	BAd	00	-	-	-	-	-	-	-	-	-	-
	Read VPB Status	1	BAd	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-
	VPB Clear	2	X	A0	BAd	01	-	-	-	-	-	-	-	-	-	-
Exit Protection Command Set(10)		2	X	90	X	00	-	-	-	-	-	-	-	-	-	-
Enter Extended Memory Block(4)		3	555	AA	2AA	55	555	88	-	-	-	-	-	-	-	-
Exit Extended Memory Block		4	555	AA	2AA	55	555	90	X	00	-	-	-	-	-	-

1. Ad = address; Dat = data; BAd = Any address in the Block; RD = Read data; PWDn = Password byte 0 to 3; PWAn = Password Address (n = 0 to 3); X = Don't care. All values in the table are in hexadecimal.
2. Grey cells represent Read cycles. The other cells are Write cycles.
3. DQ15 to DQ8 are 'Don't care' during unlock and command cycles. Amax to A16 are 'Don't care' during unlock and command cycles unless an address is required.
4. An Enter command sequence must be issued prior to any operation. It disables read and write operations from and to block 0. Read and write operations from any other block are allowed.
5. DATA = Lock Register content.
6. Only one portion of password can be programmed or read by each Password Program command.
7. The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.
8. Protected and unprotected states correspond to 00 and 01, respectively.
9. The Clear all NVPBs command programs all NVPBs before erasure in order to prevent the over-erasure of previously cleared Non-volatile Modify Protection bits.
10. If an Entry Command Set command is issued, an Exit Protection Command Set command must be issued to return the device to Read mode.

7 Registers

The device feature two registers:

1. A Lock Register that allows to configure the memory blocks and Extended Memory Block protection (see *Table 16: Block Protection Status*)
2. A Status Register that provides information on the current or previous Program or Erase operations.

7.1 Lock Register

The Lock Register is a 16-bit one-time programmable register. The bits in the Lock Register are summarized in *Table 15: Lock Register bits*.
See *Section 6.3.3: Lock Register command set* for a description of the commands allowing to read and program the Lock Register.

7.1.1 Password Protection Mode Lock bit (DQ2)

The Password Protection Mode Lock bit, DQ0, is one-time programmable. Programming (setting to ‘0’) this bit permanently places the device in Password Protection mode.

Any attempt to program the Password Protection mode Lock bit when the Non-Volatile Protection Mode bit is programmed causes the operation to abort and the device to return to Read mode.

7.1.2 Non-Volatile Protection Mode Lock bit (DQ1)

The Non-Volatile Protection Mode Lock bit, DQ1, is one-time programmable. Programming (setting to ‘0’) this bit permanently places the device in Non-Volatile Protection mode.

When shipped from Numonyx factory, all parts default to operate in Non-Volatile Protection mode. The memory blocks are unprotected (NVPBs set to ‘1’).

Any attempt to program the Non-Volatile Protection mode Lock bit when the Password Protection Mode bit is programmed causes the operation to abort and the device to return to Read mode.

7.1.3 Extended Memory Block Protection bit (DQ0)

If the device is shipped with the Extended Memory Block unlocked, the block can be protected by setting the Extended Memory Block Protection bit, DQ0, to ‘0’. However, this bit is one-time programmable and once protected the Extended Memory Block cannot be unprotected any more.

The Extended Memory Block protection status can be read in Auto Select mode either by applying V_{ID} to A9 (see *Table 7* and *Table 8*) or by issuing an Auto Select command (see *Table 9* and *Table 10*).

Table 15. Lock Register bits(1)

DQ15-3(2)	DQ2	DQ1	DQ0
Reserved	Password Protection Mode Lock bit	Non-Volatile Protection Mode Lock bit	Extended Memory Block Protection bit

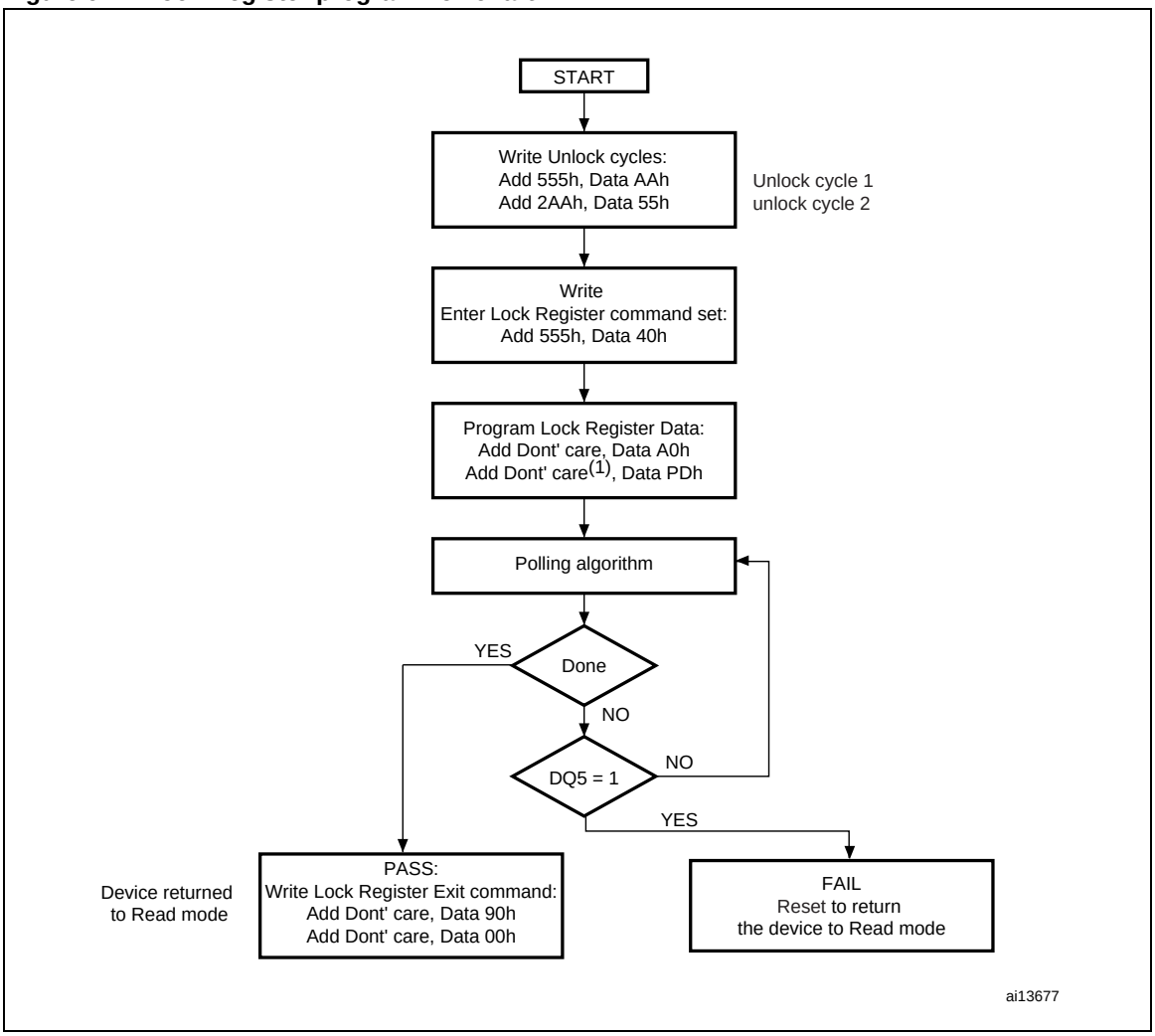
1. DQ0, DQ1 and DQ2 Lock Register bits are set to ‘1’ when shipped from the Numonyx.
2. DQ15 to DQ3 are reserved and default to ‘1’.

Table 16. Block Protection Status

NVPB Lock bit(1)	Block NVPB(2)	Block VPB(3)	Block protection status	Block Protection Status
1	1	1	00h	Block unprotected (NVPB changeable)
1	1	0	01h	Block protected by VPB (NVPB changeable)
1	0	1	01h	Block protected by NVPB (NVPB changeable)
1	0	0	01h	Block protected by NVPB and VPB (NVPB changeable)
0	1	1	00h	Block unprotected (NVPB unchangeable)
0	1	0	01h	Block protected by VPB (NVPB unchangeable)
0	0	1	01h	Block protected by NVPB (NVPB unchangeable)
0	0	0	01h	Block protected by NVPB and VPB (NVPB unchangeable)

1. If the NVPB Lock bit is set to ‘0’, all NVPBs are locked. If the NVPB Lock bit is set to ‘1’, all NVPBs are unlocked.
2. If the Block NVPB is set to ‘0’, the block is protected, if set to ‘1’, it is unprotected.
3. If the Block VPB is set to ‘0’, the block is protected, if set to ‘1’, it is unprotected.

Figure 9. Lock Register program flowchart



1. PD is the programmed data (see *Table 15: Lock Register bits*).
2. Each bit of the Lock Register can only be programmed once.

7.2 Status Register

The M29EW discrete device has one Status Register. The various bits convey information and errors on the current and previous program/erase operation. Bus Read operations from any address within the memory, always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in *Table 17: Status Register bits*.

7.2.1 Data Polling bit (DQ7)

The Data Polling bit can be used to identify whether the Program/Erase controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations, from the address just programmed, output DQ7, not its complement.

During Erase operations the Data Polling bit outputs ‘0’, the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read mode.

In Erase Suspend mode the Data Polling bit will output a ‘1’ during a Bus Read operation within a block being erased. The Data Polling bit will change from ‘0’ to ‘1’ when the Program/Erase controller has suspended the Erase operation.

Figure 10: Data polling flow chart, gives an example of how to use the Data Polling bit. A Valid Address is the address being programmed or an address within the block being erased.

7.2.2 Toggle bit (DQ6)

The Toggle bit can be used to identify whether the Program/Erase controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle bit is output on DQ6 when the Status Register is read.

During a Program/Erase operation the Toggle bit changes from ‘0’ to ‘1’ to ‘0’, etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle bit will output when addressing a cell within a block being erased. The Toggle bit will stop toggling when the Program/Erase controller has suspended the Erase operation.

Figure 11: Toggle flow chart, gives an example of how to use the Data Toggle bit.

7.2.3 Error bit (DQ5)

The Error bit can be used to identify errors detected by the Program/Erase controller. The Error bit is set to ‘1’ when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error bit is set a Read/Reset command must be issued

before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to ‘0’ back to ‘1’ and attempting to do so will set DQ5 to ‘1’. A Bus Read operation to that address will show the bit is still ‘0’. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ‘0’ to ‘1’.

7.2.4 Erase Timer bit (DQ3)

The Erase Timer bit can be used to identify the start of Program/Erase controller operation during a Block Erase command. Once the Program/Erase controller starts erasing the Erase Timer bit is set to ‘1’. Before the Program/Erase controller starts the Erase Timer bit is set to ‘0’ and additional blocks to be erased may be written to the command interface. The Erase Timer bit is output on DQ3 when the Status Register is read.

7.2.5 Alternative Toggle bit (DQ2)

The Alternative Toggle bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle bit changes from ‘0’ to ‘1’ to ‘0’, etc., with successive Bus Read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle bit changes from ‘0’ to ‘1’ to ‘0’, etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory array data as if in Read mode.

After an Erase operation that causes the Error bit to be set, the Alternative Toggle bit can be used to identify which block or blocks have caused the error. The Alternative Toggle bit changes from ‘0’ to ‘1’ to ‘0’, etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle bit does not change if the addressed block has erased correctly.

7.2.6 Buffered Program Abort bit (DQ1)

The Buffered Program Abort bit, DQ1, is set to ‘1’ when a Buffer Program operation aborts. The Buffered Program Abort and Reset command must be issued to return the device to Read mode (see Write to Buffer Program in *Section 6.1: Standard commands*).

For the complete polling flow chart, please refer to *Figure 12.: Status Register Polling Flow Chart*.

Table 17. Status Register bits(1)

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#
Program(2)	Any address	$\overline{DQ7}$	Toggle	0	–	No Toggle	0	0
Program During Erase Suspend	Any address	$\overline{DQ7}$	Toggle	0	–	–	–	0
Buffered Program Abort(2)	Any address	$\overline{DQ7}$	Toggle	0	–	–	1	0
Program Error	Any address	$\overline{DQ7}$	Toggle	1	–	–	–	Hi-Z
Chip Erase	Any address	0	Toggle	0	1	Toggle	–	0
Block Erase before timeout	Erasing block	0	Toggle	0	0	Toggle	–	0
	Non-erasing block	0	Toggle	0	0	No toggle	–	0
Block Erase	Erasing block	0	Toggle	0	1	Toggle	–	0
	Non-erasing block	0	Toggle	0	1	No toggle	–	0
Erase Suspend	Erasing block	1	No Toggle	0	–	Toggle	–	Hi-Z
	Non-erasing block	Data read as normal					–	Hi-Z
Erase Error	Good block address	0	Toggle	1	1	No toggle	–	Hi-Z
	Faulty Block address	0	Toggle	1	1	Toggle	–	Hi-Z

1. Unspecified data bits should be ignored.
2. $\overline{DQ7}$ for Buffer Program is related to the last address location loaded.

Figure 10. Data polling flow chart

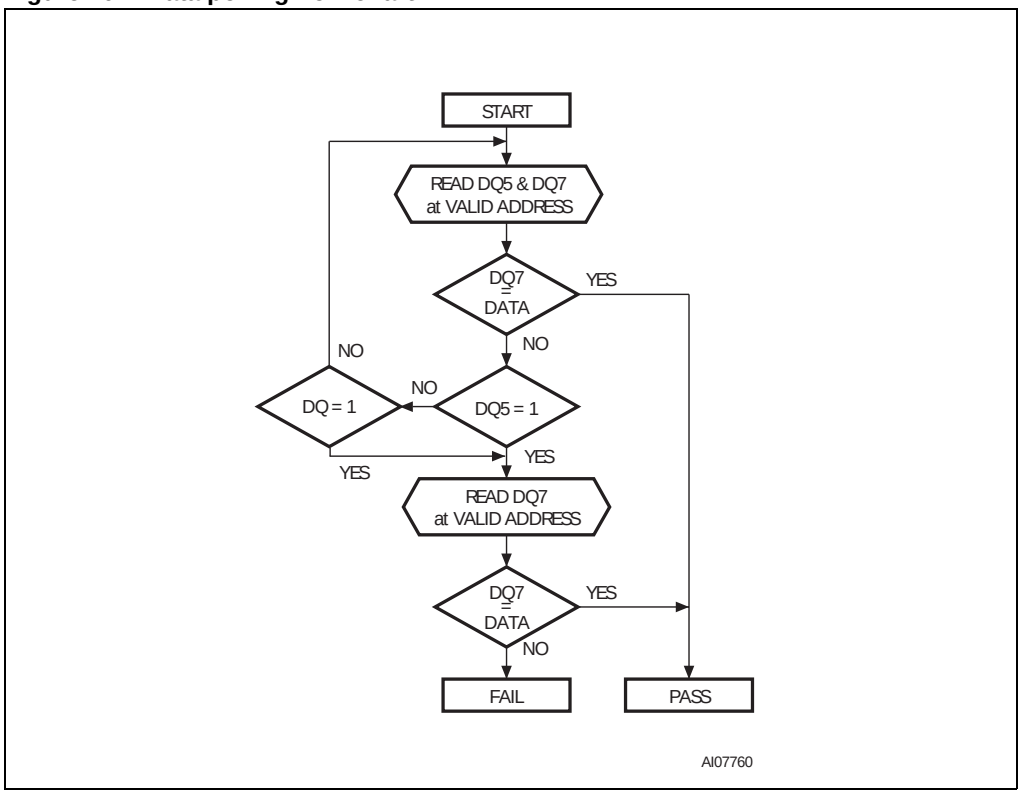


Figure 11. Toggle flow chart

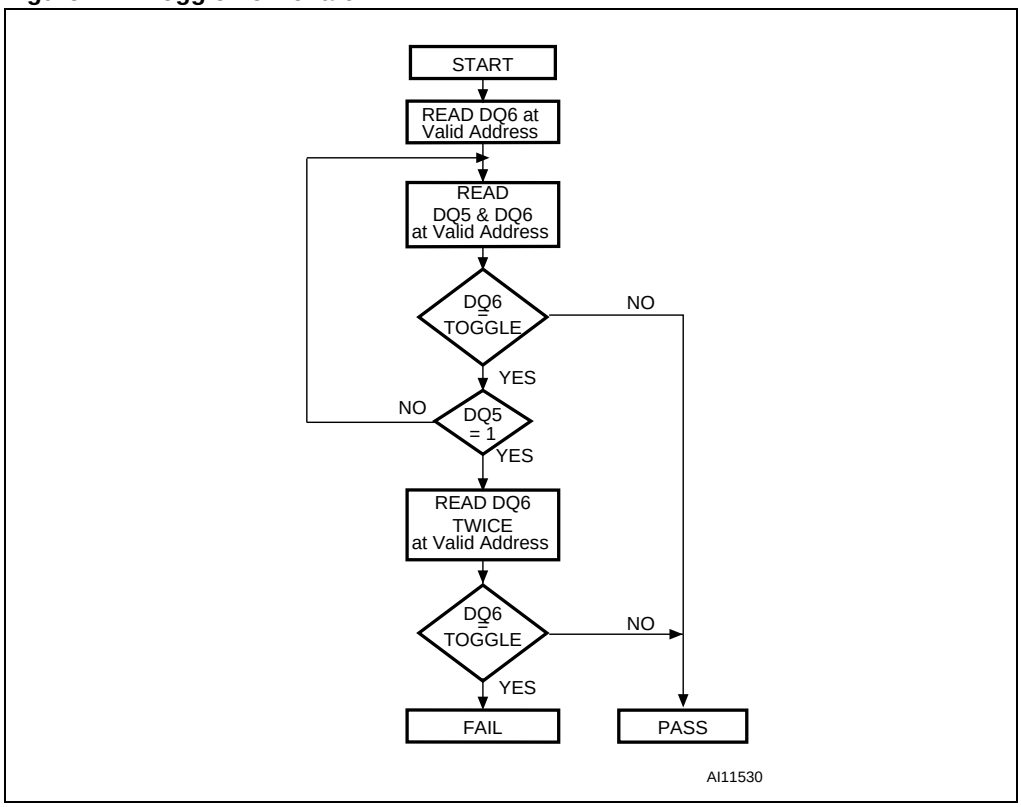
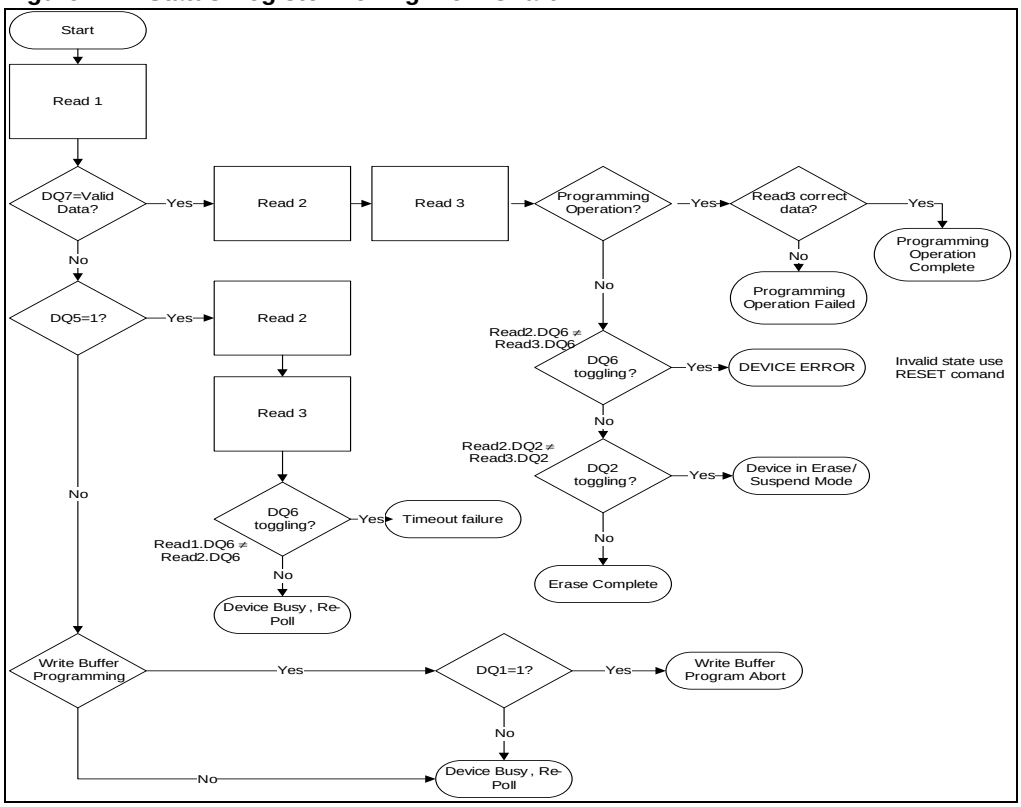


Figure 12. Status Register Polling Flow Chart



8 Maximum Ratings

Stressing the device above the rating listed in *Table 18: Absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Refer also to the relevant quality documents from Numonyx.

Table 18. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature under bias	–50	125	°C
T_{STG}	Storage temperature	–65	150	°C
V_{IO}	Input or output voltage(1)(2)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.6	4	V
V_{CCQ}	Input/output supply voltage	–0.6	4	V
V_{PPH}(3)	Program voltage	–0.6	14.5	V

1. Minimum voltage may undershoot to –2 V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to V_{CC} + 2 V during transition and for less than 20ns during transitions.
3. V_{PPH} must not remain at 12 V for more than a total of 80hrs.

9 DC and AC Parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 19: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 19. Operating and AC measurement conditions

Parameter	Min	Max	Unit
V_{CC} supply voltage	2.7	3.6	V
V_{CCQ} supply voltage ($V_{CCQ} \le V_{CC}$)	1.65	3.6	V
V_{PP} supply voltage	-2.0	12.5	V
Ambient operating temperature	– 40	85	°C
Load capacitance (C_L)	30		pF
Input rise and fall times		10	ns
Input pulse voltages	0 to V_{CCQ}		V
Input and output timing ref. voltages	$V_{CCQ}/2$		V

Figure 13. AC measurement load circuit

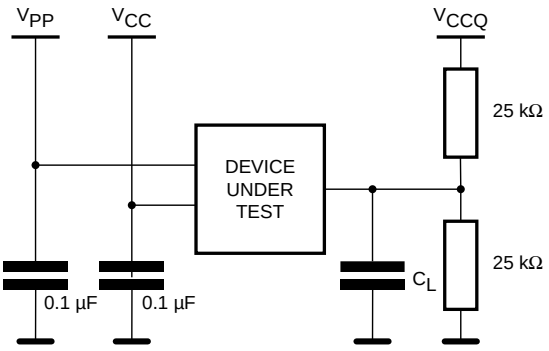


Figure 14. AC measurement I/O waveform

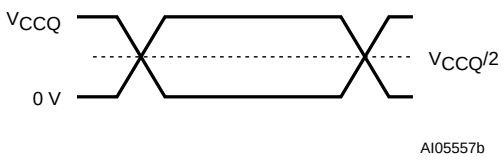


Table 20. Power-up wait timings

Symbol	Alt.	Parameter	Min	Unit
$t_{VCHVCQH}$	-	V_{CC}(1) High to V_{CCQ}(1) High	0	µs
t_{VCHPH}(2)	t_{VCS}	V_{CC} High to rising edge of RST#	300	µs
t_{VCQHPH}(2)	t_{VIOS}	V_{CCQ} High to rising edge of RST#	0	µs
t_{PHEL}	t_{RH}	RST# High to Chip Enable Low	50	ns
t_{PHWL}	-	RST# High to Write Enable Low	150	ns

1. V_{CC} and V_{CCQ} ramps must be synchronized during power-up.
2. If RST# is not stable for t_{VCHRH} or t_{VCQHRH}, the device does not permit any Read and Write operations and a hardware reset is required.

Figure 15. Power-up wait timings

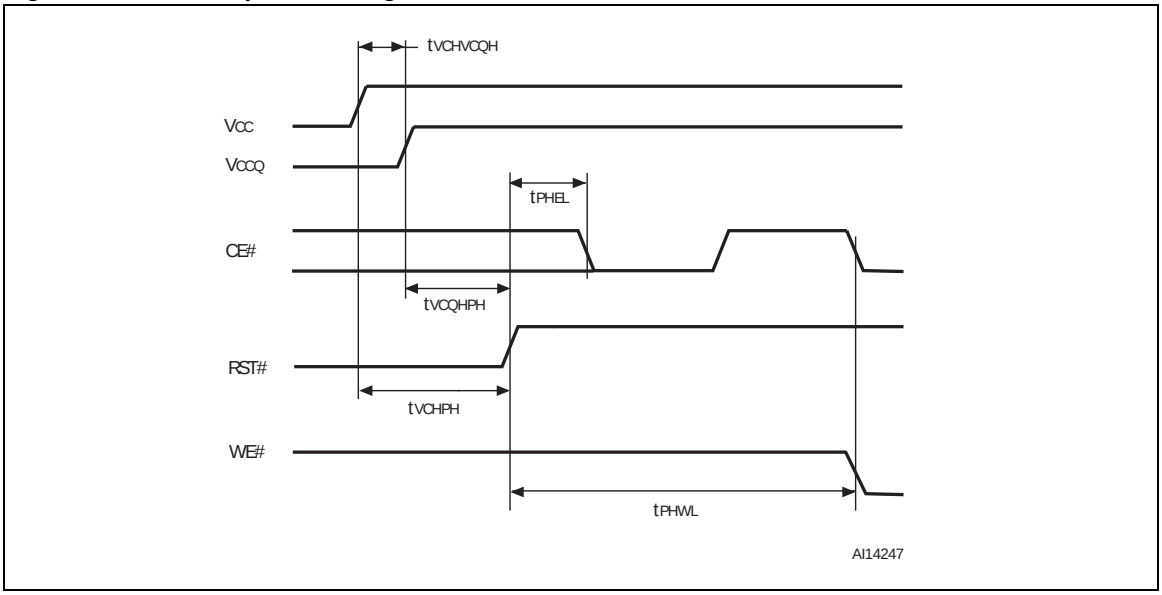


Table 21. Device capacitance(1)

Symbol	Parameter	Test condition	Min	Max	Unit
C_{IN}	Input capacitance for 256-Mbit and 512-Mbit	V_{IN} = 0 V	3	8	pF
	Input capacitance for 1-Gbit		4	9	
	Input capacitance for 2-Gbit (1-Gbit/1-Gbit)		8	18	
C_{OUT}	Output capacitance	V_{OUT} = 0 V	3	6	

1. Sampled only, not 100% tested.

Table 22. DC characteristics

Symbol	Parameter		Test condition		Min	Typ	Max	Unit
I_{LI}(1)	Input leakage current		0 V ≤ V_{IN} ≤ V_{CC}		-	-	±1	µA
I_{LO}	Output leakage current		0 V ≤ V_{OUT} ≤ V_{CC}		-	-	±1	µA
I_{CC1}	Read current	Random Read	CE# = V_{IL}, OE# = V_{IH}, f = 5 MHz		-	26	31	mA
		Page Read	CE# = V_{IL}, OE# = V_{IH}, f = 13 MHz		-	12	16	mA
I_{CC2}	Supply current (Standby)	256-Mbit	CE# = V_{CCQ} ± 0.2 V, RST# = V_{CCQ} ± 0.2 V		-	65	210	µA
		512-Mbit			-	70	225	
		1-Gbit			-	75	240	
		2-Gbit			-	150	480	
I_{CC3}(2)	Supply current (Program/Erase)		Program/Erase controller active	V_{PP}/WP# = V_{IL} or V_{IH}	-	35	50	mA
				V_{PP}/WP#=V_{PPH}	-	35	50	mA
I_{PP1}	V_{PP} current	Read	V_{PP}/WP# ≤ V_{CC}		-	0.2	5	µA
		Standby	V_{PP}/WP# ≤ V_{CC}		-	2	15	µA
I_{PP2}		Reset	RST# = V_{SS} ± 0.2 V		-	0.2	5	µA
I_{PP3}		Program operation ongoing	V_{PP}/WP# = 12 V ± 5%		-	0.05	0.10	mA
			V_{PP}/WP# = V_{CC}		-	0.05	0.10	mA
I_{PP4}		Erase operation ongoing	V_{PP}/WP# = 12 V ± 5%		-	0.05	0.10	mA
			V_{PP}/WP# = V_{CC}		-	0.05	0.10	mA
V_{IL}	Input Low voltage		V_{CC} ≥ 2.7 V		–0.5	-	0.8	V
V_{IH}	Input High voltage		V_{CC} ≥ 2.7 V		0.7V_{CCQ}	-	V_{CCQ}+0.4	V
V_{OL}	Output Low voltage		I_{OL} = 100 µA, V_{CC} = $V_{CC(min)}$, V_{CCQ} = $V_{CCQ(min)}$		-	-	0.15V_{CCQ}	V
V_{OH}	Output High voltage		I_{OH} = 100 µA, V_{CC} = $V_{CC(min)}$, V_{CCQ} = $V_{CCQ(min)}$		0.85V_{CCQ}	-	-	V
V_{PPLK}	V_{PP} Lock-Out voltage		-		-	-	0.4	V
V_{PPH}	Voltage for V_{PP}/WP# Program acceleration		-		11.5	-	12.5	V
V_{LKO}(2)	Program/Erase lockout supply voltage		-		2.3	-	-	V

1. The maximum input leakage current is ±5 µA on the V_{PP}/WP# pin.
2. Sampled only, not 100% tested.

Figure 16. Random Read AC waveforms (8-bit mode)

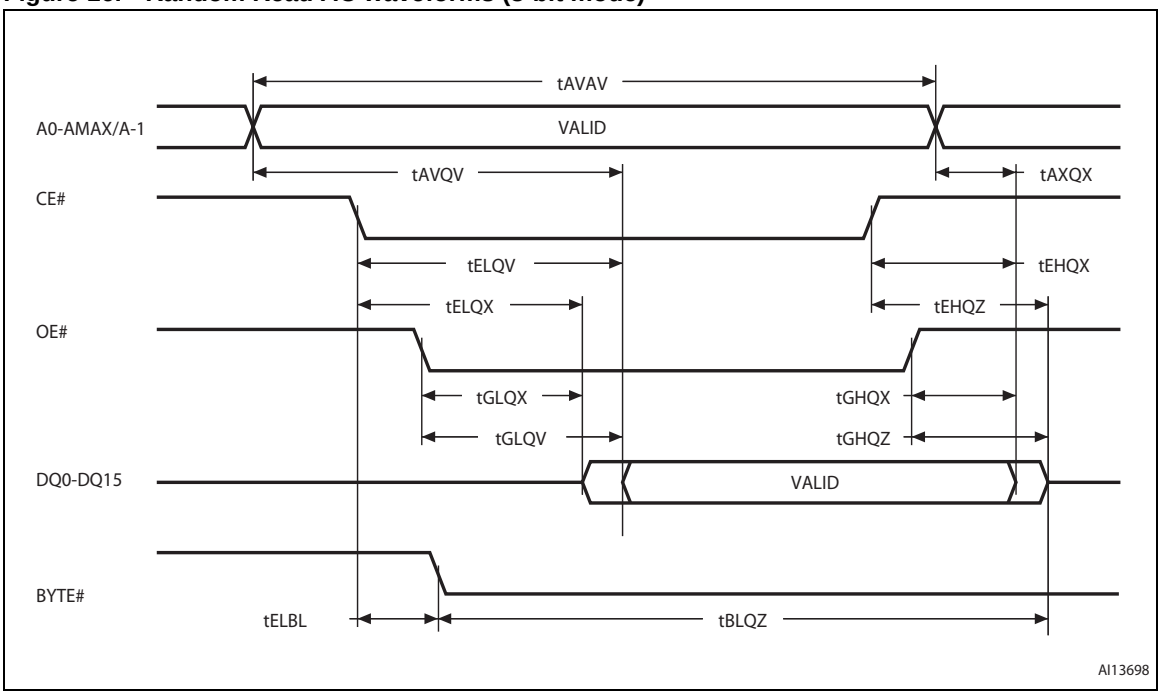


Figure 17. Random Read AC waveforms (16-bit mode)

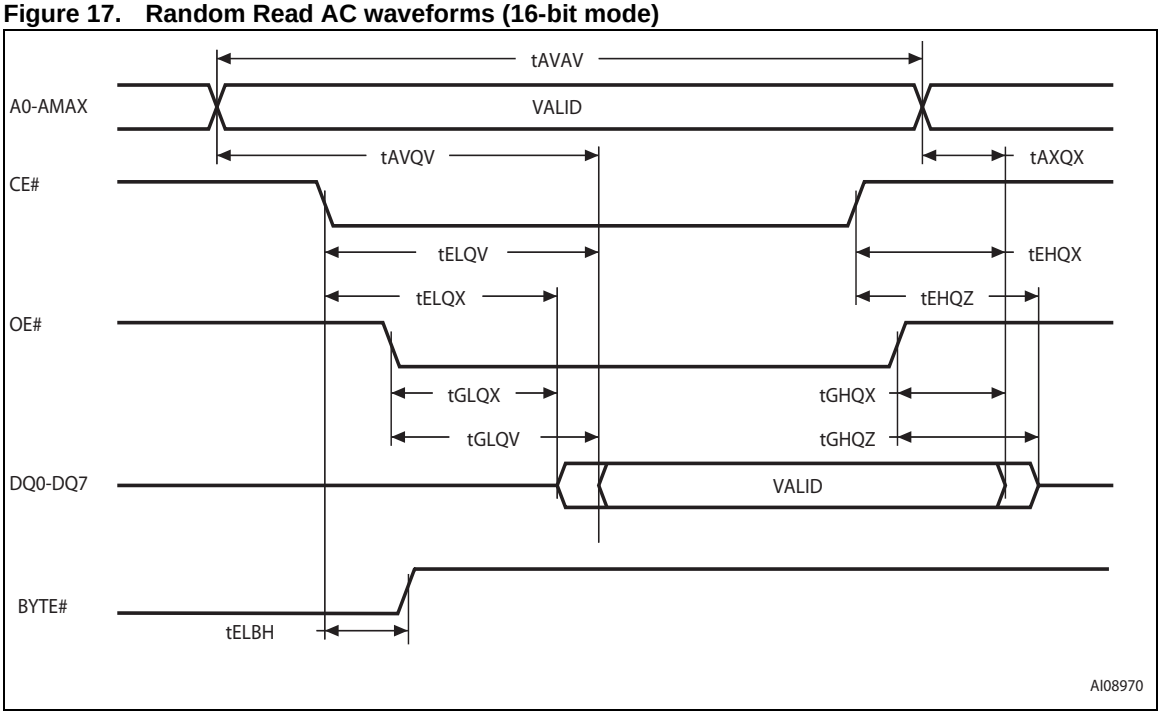


Figure 18. BYTE# Transition AC Waveform

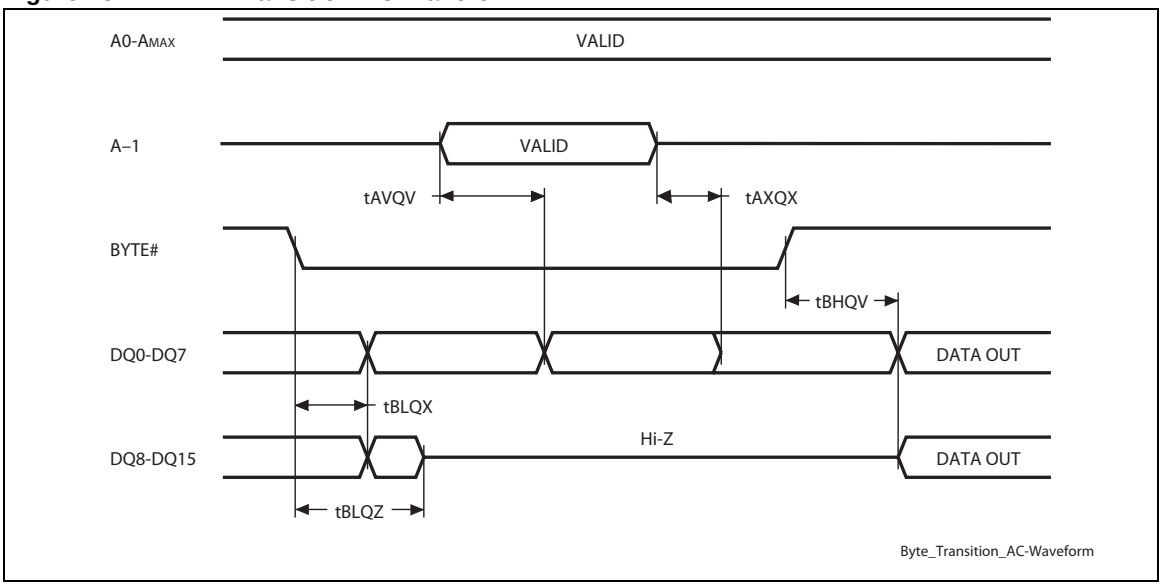


Figure 19. Page Read AC waveforms (16-bit mode)

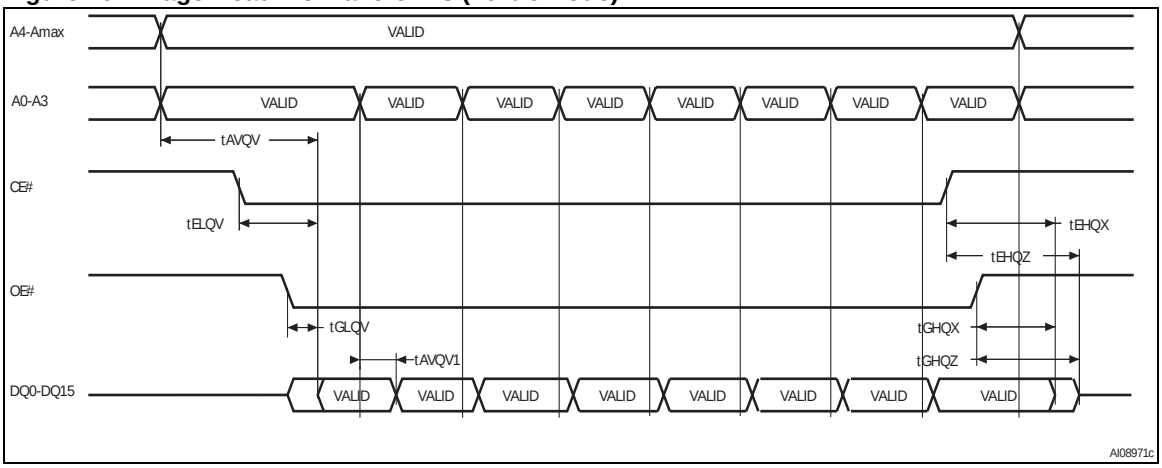


Table 23. Read AC characteristics

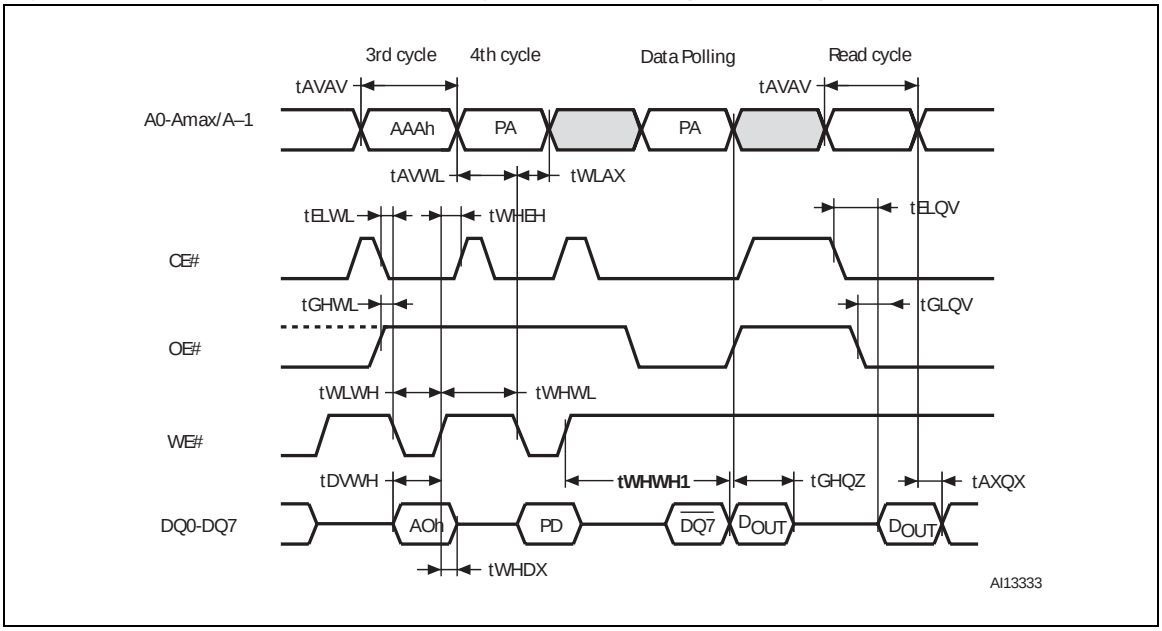
Symbol	Alt.	Parameter	Test condition	Limit	M29EW		Unit
					Fortified BGA	TSOP	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	CE# = V_{IL}, OE# = V_{IL}	Min	100	110	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	CE# = V_{IL}, OE# = V_{IL}	Max	100	110	ns
t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	CE# = V_{IL}, OE# = V_{IL}	Max	25		ns
t_{ELQX}(1)	t_{LZ}	Chip Enable Low to Output Transition	OE# = V_{IL}	Min	0		ns

Table 23. Read AC characteristics

Symbol	Alt.	Parameter	Test condition	Limit	M29EW		Unit
					Fortified BGA	TSOP	
t_{ELQV}	t_E	Chip Enable Low to Output Valid	OE# = V_{IL}	Max	100	110	ns
t_{GLQX}(1)	t_{OLZ}	Output Enable Low to Output Transition	CE# = V_{IL}	Min	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	CE# = V_{IL}	Max	25		ns
t_{EHQZ}(1)	t_{HZ}	Chip Enable High to Output Hi-Z	OE# = V_{IL}	Max	20		ns
t_{GHQZ}(1)	t_{DF}	Output Enable High to Output Hi-Z	CE# = V_{IL}	Max	15		ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition	-	Min	0		ns
t_{ELBL} t_{ELBH}	t_{ELFL} t_{ELFH}	Chip Enable to BYTE# Low or High	-	Max	10		ns
t_{BLQV}	t_{FLQV}	BYTE# Low to Output Valid	-	Max	1		µs
t_{BHQV}	t_{FHQV}	BYTE# High to Output Valid	-	Max	1		µs

1. Sampled only, not 100% tested.

Figure 20. Write Enable Controlled Program waveforms (8-bit mode)

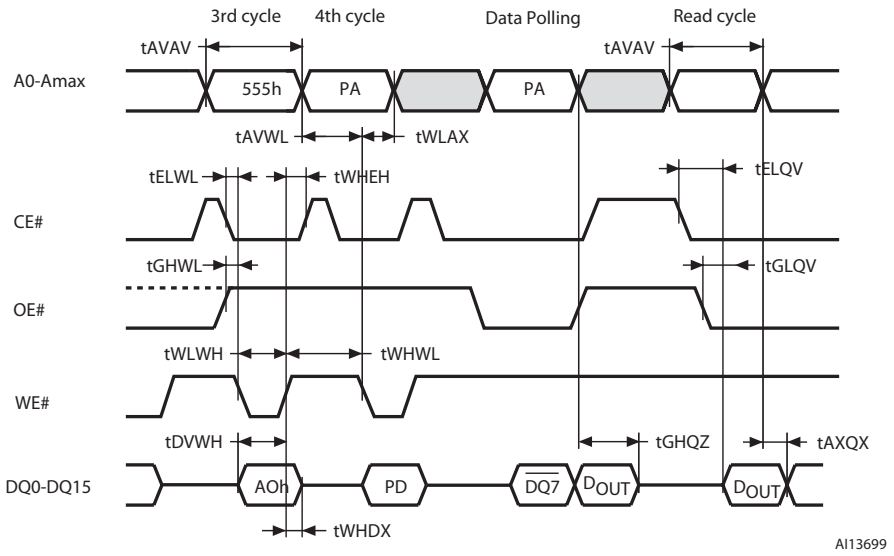


1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of Status Register Data Polling bit and by a read operation that outputs the data, DOUT, programmed by the previous

Program command.

2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.2.1: Data Polling bit (DQ7)*).
4. See*Table 24: Write AC characteristics, Write Enable Controlled*, *Table 25: Write AC characteristics, Chip Enable Controlled* and *Table 23: Read AC characteristics* for details on the timings.

Figure 21. Write Enable Controlled Program waveforms (16-bit mode)



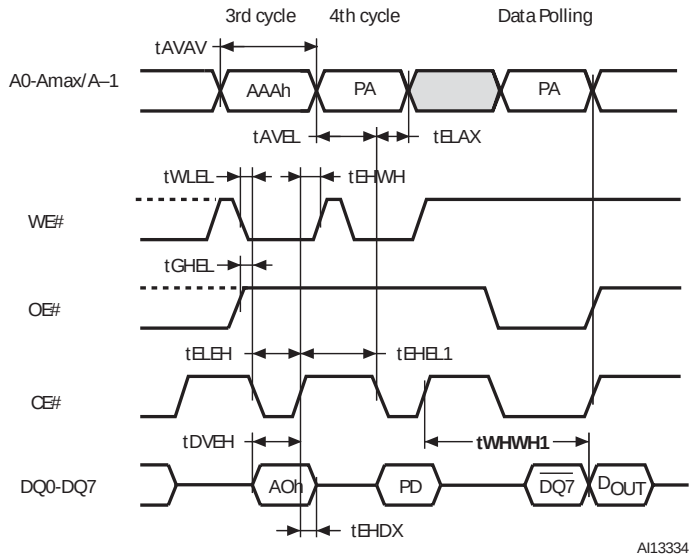
1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of Status Register Data Polling bit and by a read operation that outputs the data, DOUT, programmed by the previous Program command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.2.1: Data Polling bit (DQ7)*).
4. See*Table 24: Write AC characteristics, Write Enable Controlled*, *Table 25: Write AC characteristics, Chip Enable Controlled* and *Table 23: Read AC characteristics* for details on the timings.

Table 24. Write AC characteristics, Write Enable Controlled

Symbol	Alt	Parameter	Limit	Fortified BGA	TSOP	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	100	110	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	35		ns
t_{DVWH}(1)	t_{DS}	Input Valid to Write Enable High	Min	30		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	45		ns
t_{GHWL}	-	Output Enable High to Write Enable Low	Min	0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0		ns
t_{WHRL}(2)	t_{BUSY}	Program/Erase Valid to RY/BY# Low	Max	30		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	300		µs

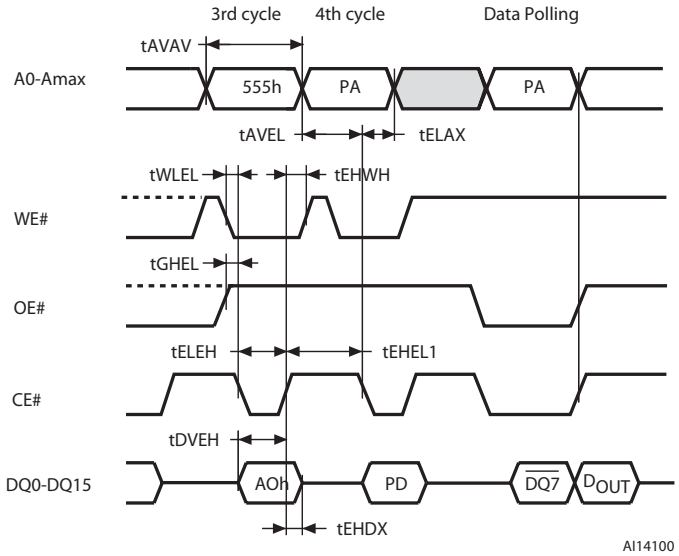
1. This specification must be complied with by customer's writing timing. Any violation to this timing specification may damage the flash device permanently.
2. Sampled only, not 100% tested.

Figure 22. Chip Enable Controlled Program waveforms (8-bit mode)



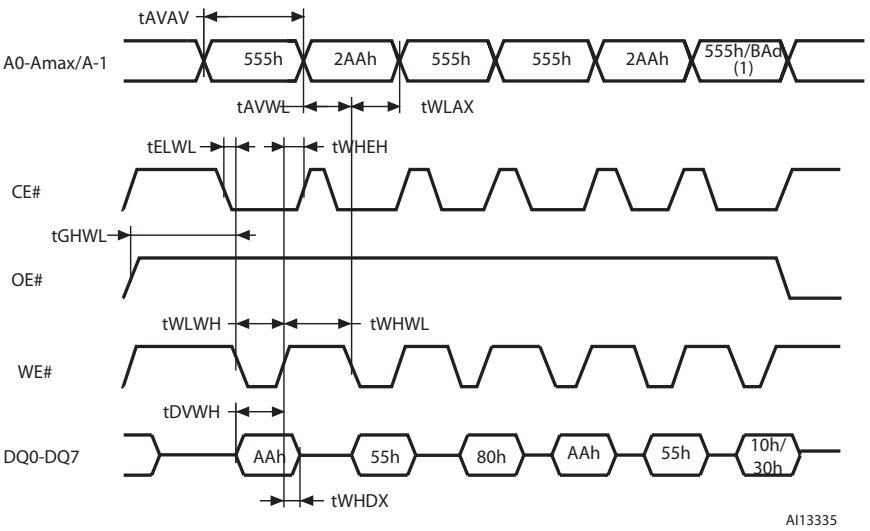
1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of Status Register Data Polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.2.1: Data Polling bit (DQ7)*).
4. See *Table 24: Write AC characteristics, Write Enable Controlled*, *Table 25: Write AC characteristics, Chip Enable Controlled* and *Table 23: Read AC characteristics* for details on the timings.

Figure 23. Chip Enable Controlled Program waveforms (16-bit mode)



1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of Status Register Data Polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.2.1: Data Polling bit (DQ7)*).
4. See *Table 24: Write AC characteristics, Write Enable Controlled*, *Table 25: Write AC characteristics, Chip Enable Controlled* and *Table 23: Read AC characteristics* for details on the timings.

Figure 24. Chip/Block Erase waveforms (8-bit mode)



1. For a Chip Erase command, addresses and data are 555h and 10h, respectively, while they are BAd and 30h for a Block Erase command.
2. BAd is the block address.
3. See *Table 24: Write AC characteristics, Write Enable Controlled*, *Table 25: Write AC characteristics, Chip Enable Controlled* and *Table 23: Read AC characteristics* for details on the timings.

Table 25. Write AC characteristics, Chip Enable Controlled

Symbol	Alt.	Parameter	Limit	Fortified BGA	TSOP	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	100	110	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	35		ns
t_{DVEH} (1)	t_{DS}	Input Valid to Chip Enable High	Min	30		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	45		ns
t_{GHEL}	-	Output Enable High Chip Enable Low	Min	0		ns

1. This specification must be complied with by customer's writing timing. The result would be unpredictable if there's any violation to this timing specification.

Figure 25. Reset AC waveforms (no program/erase in progress)

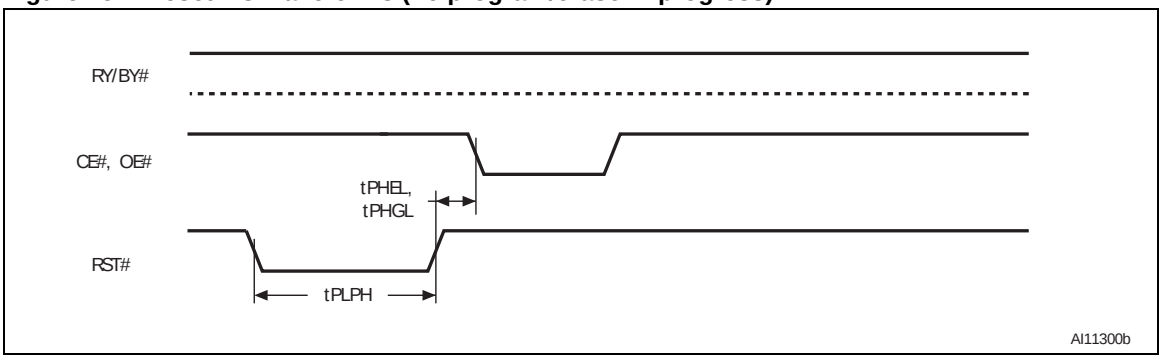


Figure 26. Reset during program/erase operation AC waveforms

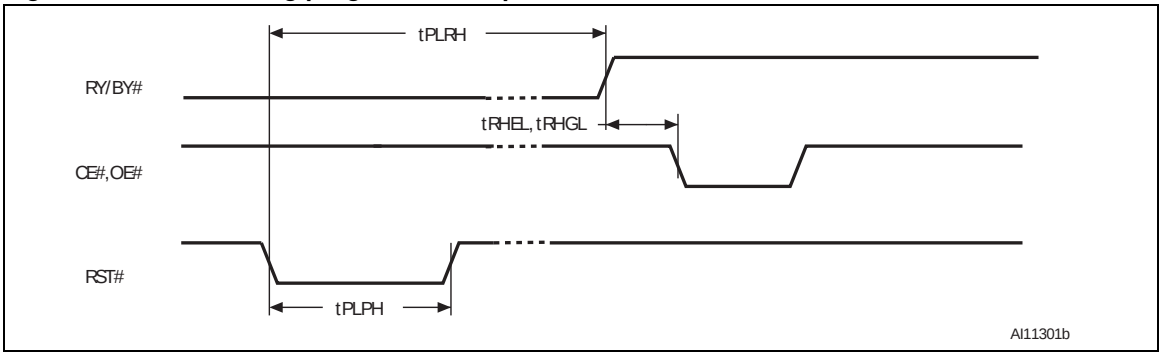


Table 26. Reset AC characteristics

Symbol	Alt.	Parameter	Min	Max	Unit
t_{PLRH} (1)	t_{READY}	RST# Low to Read mode, during Program or Erase	-	32	µs
t_{PLPH}	t_{RP}	RST# Pulse width	100	-	ns
t_{PHEL}, t_{PHGL} (1)	t_{RH}	RST# High to Write Enable Low, Chip Enable Low, Output Enable Low	50	-	ns
-	t_{RPD}	RST# Low to Standby mode, during Read mode	10	-	µs
		RST# Low to Standby mode, during Program or Erase	50	-	µs
t_{RHEL}, t_{RHGL} (1)	t_{RB}	RY/BY# High to Write Enable Low, Chip Enable Low, Output Enable Low	0	-	ns

1. Sampled only, not 100% tested.

Figure 27. Accelerated program timing waveforms

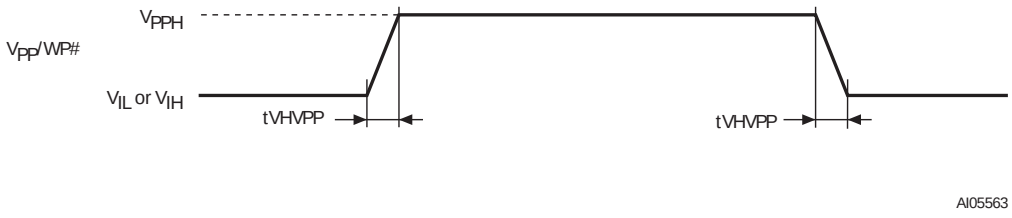
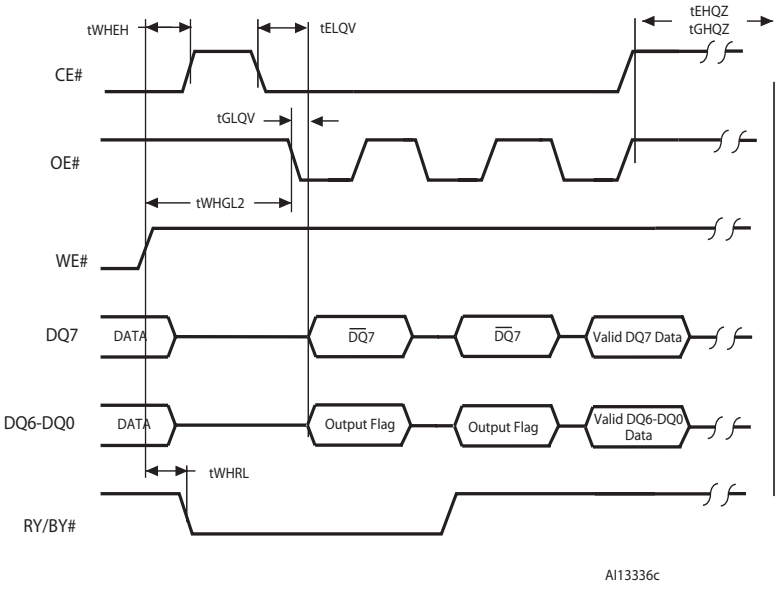
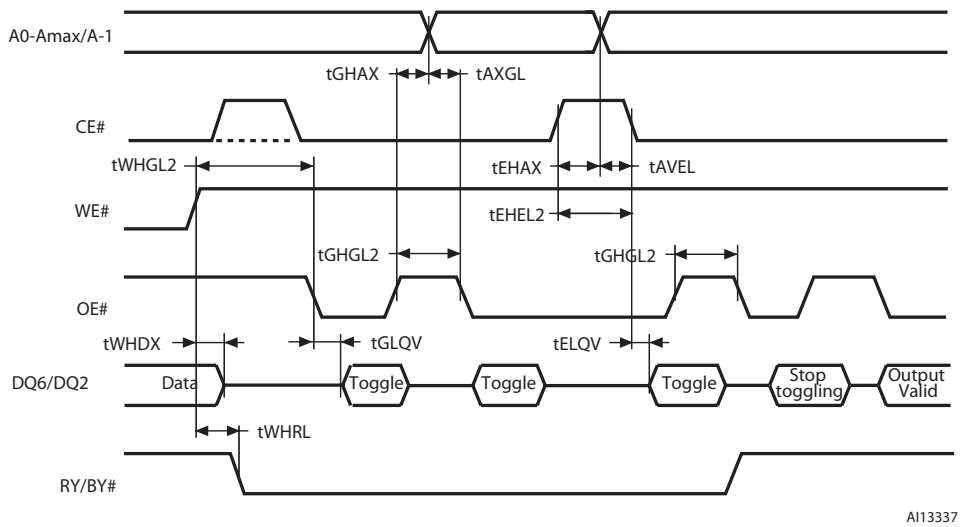


Figure 28. Data polling AC waveforms



1. DQ7 returns valid data bit when the ongoing Program or Erase command is completed.
2. See *Table 27: Accelerated Program and Data Polling/Data Toggle AC characteristics* and *Table 23: Read AC characteristics* for details on the timings.

Figure 29. Toggle/Alternative Toggle bit polling AC waveforms (8-bit mode)



1. DQ6 stops toggling when the ongoing Program or Erase command is completed. DQ2 stops toggling when the in-progress Chip Erase or Block Erase command is completed.
2. See *Table 27: Accelerated Program and Data Polling/Data Toggle AC characteristics* and *Table 23: Read AC characteristics* for details on the timings.

Table 27. Accelerated Program and Data Polling/Data Toggle AC characteristics

Symbol	Alt	Parameter	Min	Max	Unit
t_{VHVPP}	-	V_{PP}/WP# raising or falling time	250	-	ns
t_{AXGL}	t_{ASO}	Address setup time to Output Enable Low during Toggle bit polling	15	-	ns
t_{GHAX}, t_{EHAX}	t_{AHT}	Address hold time from Output Enable during Toggle bit polling	0	-	ns
t_{EHEL2}	t_{EPH}	Chip Enable High during Toggle bit polling	30	-	ns
t_{WHGL2}, t_{GHGL2}	t_{OEH}	Output Hold time during Data and Toggle bit polling	20	-	ns
t_{WHRL}	t_{BUSY}	Program/Erase Valid to RY/BY# Low	-	90	ns

10 Programming and Erase Performance

Table 28. Programming and Erase Performance

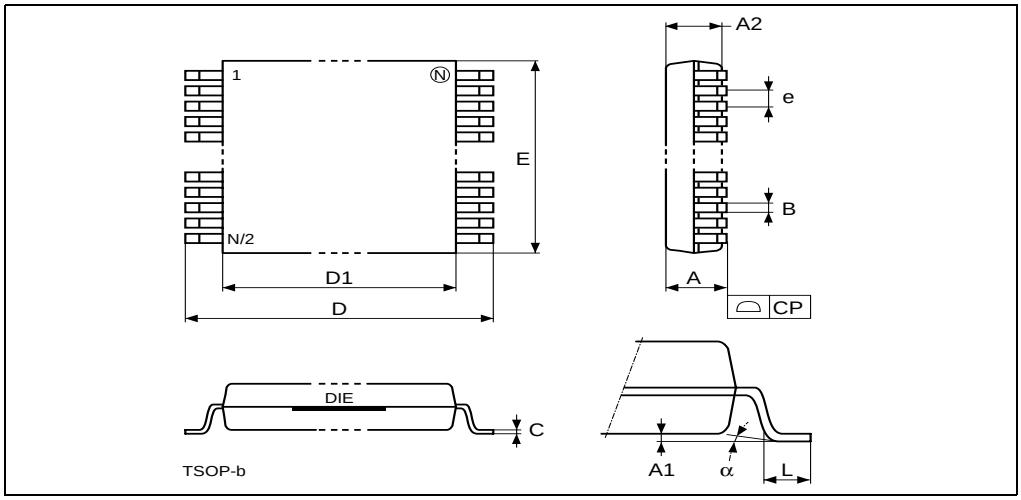
Parameter		Buffer Size	Byte	Word	Min	Typ(1)(2)	Max(2)	Unit
Block Erase (128 kbytes)		-	-	-	-	0.8	4	s
Erase Suspend latency time		-	-	-	-	27	32	µs
Block Erase time-out		-	-	-	50	-	-	µs
Byte Program	Single Byte Program	-	-	-	-	210	456	µs
	Byte Write to Buffer Program	64	64	-	-	270	716	µs
		128	128	-	-	310	900	
		256	256	-	-	375	1140	
	Effective Write to Buffer Program per Byte	64	1	-	-	4.22	11.2	µs
		128	1	-	-	2.42	7.00	
		256	1	-	-	1.46	4.45	
Word Program	Single Word Program	-	-	-	-	210	456	µs
	Word Write to Buffer Program	32	-	32	-	270	716	µs
		64	-	64	-	310	900	
		128	-	128	-	375	1140	
		256	-	256	-	505	1690	
		512	-	512	-	900	3016	
	Effective Write to Buffer Program per Word	32	-	1	-	8.44	22.4	µs
		64	-	1	-	4.84	14.1	
		128	-	1	-	2.93	8.90	
		256	-	1	-	1.97	6.60	
		512	-	1	-	1.76	5.89	
Program Suspend latency time		-	-	-	-	27	32	µs
Program/Erase cycles (per block)		-	-	-	100,000	-	-	Cycles
Erase to Suspend(3)		-	-	-	-	500	-	µs

1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Erase to Suspend is a typical time between an initial block erase or erase resume command and the a subsequent erase suspend command. Violating the specification repeatedly during any particular block erase may cause erase failures.

11 Package Mechanical Specifications

Numonyx offers these devices in lead-free TSOP, lead-free Fortified BGA, and leaded Fortified BGA packages. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 30. TSOP56 – 56 lead thin small-outline package, 14 x 20 mm, package outline

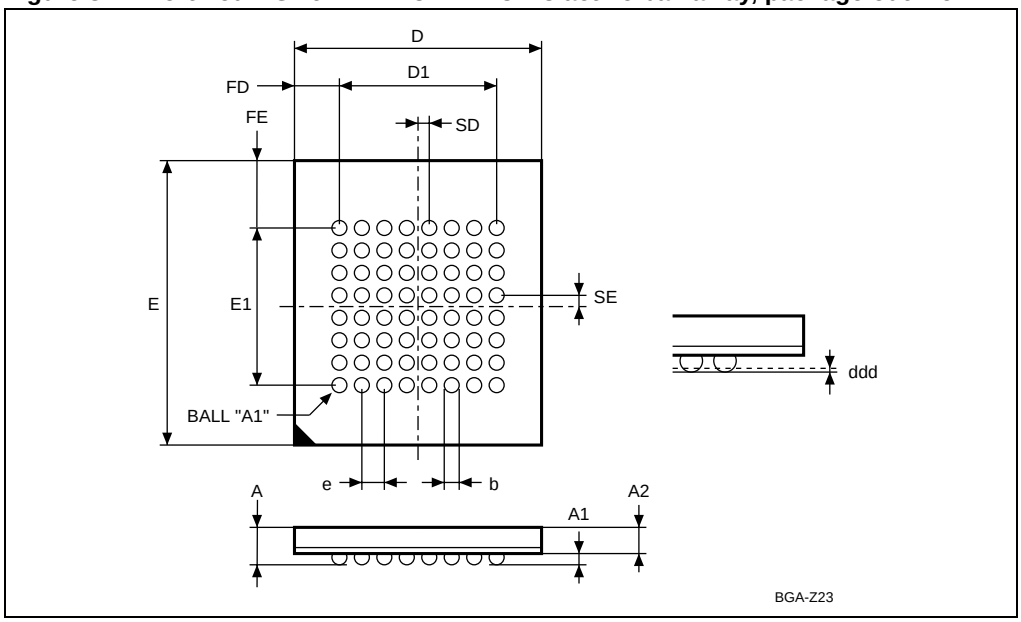


1. Drawing is not to scale.

Table 29. TSOP56 – 56 lead thin small-outline package, 14 x 20 mm, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.20	–	–	0.047
A1	0.10	0.05	0.15	0.004	0.002	0.006
A2	1.00	0.95	1.05	0.039	0.037	0.041
B	0.22	0.10	0.27	0.009	0.007	0.011
C	–	0.10	0.21	–	0.004	0.008
CP	–	–	0.10	–	–	0.004
E	14.00	13.90	14.10	0.551	0.547	0.555
D	20.00	19.80	20.20	0.787	0.780	0.795
D1	18.40	18.30	18.50	0.724	0.720	0.728
e	0.50	–	–	0.020	–	–
L	0.60	0.50	0.70	0.024	0.020	0.028
α	3	0	5	3	0	5

Figure 31. Fortified BGA64 11 x 13 mm - 8 x 8 active ball array, package outline



1. Drawing is not to scale.
2. Drawing is bottom view.

Table 30. Fortified BGA64 11 x 13 mm - 8 x 8 active ball array, package mechanical data

Symbol	millimeters		
	Typ	Min	Max
A	–	–	1.40
A1	0.49	0.40	–
A2	0.80	–	–
b	0.60	0.55	0.65
D	11.00	10.90	11.10
D1	7.00	–	–
ddd	–	–	0.10
e	1.00	–	–
E	13.00	12.90	13.10
E1	7.00	–	–
FD	2.00	–	–
FE	3.00	–	–
SD	0.50	–	–
SE	0.50	–	–

12 Ordering Information

Table 31. Ordering information scheme

Example: RC 28F 256 M29EW H *

Package

RC = Fortified BGA64: 11 x 13 mm, leaded

JS = TSOP56: 14 x 20 mm, lead free, halogen free, RoHS compliant

PC = Fortified BGA64: 11 x 13 mm, lead free, halogen free, RoHS compliant

Discrete/SCSP

28F= NOR Parallel Interface

Device Density

256=256-Mbit

512=512-Mbit

00A=1-Gbit

00B=2-Gbit

Device Type

M29EW = 3V core, page, uniform block flash memory

Device function

H = highest block protected by V_{PP}/WP#

L = lowest block protected by V_{PP}/WP#

Device features

* = Random digit to cover a combination of features, including packing media, special features, and specific customer request information.

Note: This product is also available with the Extended Memory Block Numonyx pre-locked. For further details and ordering information contact your nearest Numonyx sales office.

Devices are shipped from Numonyx factory with the memory content bits erased to '1'. For a list of available options (package, High/Low protect, etc.) or for further information on any aspect of the device, please contact your nearest Numonyx Sales Office.

Table 32. Valid Combinations of M29EW Part Numbers

256-Mbit	512-Mbit	1-Gbit	2-Gbit
JS28F256M29EWH*	JS28F512M29EWH*	JS28F00AM29EWH*	JS28F00BM29EWH*
JS28F256M29EWL*	JS28F512M29EWL*	JS28F00AM29EWL*	PC28F00BM29EWH*
PC28F256M29EWH*	PC28F512M29EWH*	PC28F00AM29EWH*	RC28F00BM29EWH*
PC28F256M29EWL*	PC28F512M29EWL*	PC28F00AM29EWL*	
RC28F256M29EWH*	RC28F512M29EWH*	RC28F00AM29EWH*	
RC28F256M29EWL*	RC28F512M29EWL*	RC28F00AM29EWL*	

Note: For further information on ordering products or for product part numbers, go to: http://www.numonyx.com/en-US/MemoryProducts/Pages/PartNumberLookup.aspx.

Appendix A Memory Address Table

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
0	128 / 64	0000000-001FFFF	0000000-000FFFF
1	128 / 64	0020000-003FFFF	0010000-001FFFF
2	128 / 64	0040000-005FFFF	0020000-002FFFF
3	128 / 64	0060000-007FFFF	0030000-003FFFF
4	128 / 64	0080000-009FFFF	0040000-004FFFF
5	128 / 64	00A0000-00BFFFF	0050000-005FFFF
6	128 / 64	00C0000-00DFFFF	0060000-006FFFF
7	128 / 64	00E0000-00FFFFF	0070000-007FFFF
8	128 / 64	0100000-011FFFF	0080000-008FFFF
9	128 / 64	0120000-013FFFF	0090000-009FFFF
10	128 / 64	0140000-015FFFF	00A0000-00AFFFF
11	128 / 64	0160000-017FFFF	00B0000-00BFFFF
12	128 / 64	0180000-019FFFF	00C0000-00CFFFF
13	128 / 64	01A0000-01BFFFF	00D0000-00DFFFF
14	128 / 64	01C0000-01DFFFF	00E0000-00EFFFF
15	128 / 64	01E0000-01FFFFF	00F0000-00FFFFF
16	128 / 64	0200000-021FFFF	0100000-010FFFF
17	128 / 64	0220000-023FFFF	0110000-011FFFF
18	128 / 64	0240000-025FFFF	0120000-012FFFF
19	128 / 64	0260000-027FFFF	0130000-013FFFF
20	128 / 64	0280000-029FFFF	0140000-014FFFF
21	128 / 64	02A0000-02BFFFF	0150000-015FFFF
22	128 / 64	02C0000-02DFFFF	0160000-016FFFF
23	128 / 64	02E0000-02FFFFF	0170000-017FFFF
24	128 / 64	0300000-031FFFF	0180000-018FFFF
25	128 / 64	0320000-033FFFF	0190000-019FFFF
26	128 / 64	0340000-035FFFF	01A0000-01AFFFF
27	128 / 64	0360000-037FFFF	01B0000-01BFFFF
28	128 / 64	0380000-039FFFF	01C0000-01CFFFF
29	128 / 64	03A0000-03BFFFF	01D0000-01DFFFF
30	128 / 64	03C0000-03DFFFF	01E0000-01EFFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
31	128 / 64	03E0000-03FFFFF	01F0000-01FFFFF
32	128 / 64	0400000-041FFFF	0200000-020FFFF
33	128 / 64	0420000-043FFFF	0210000-021FFFF
34	128 / 64	0440000-045FFFF	0220000-022FFFF
35	128 / 64	0460000-047FFFF	0230000-023FFFF
36	128 / 64	0480000-049FFFF	0240000-024FFFF
37	128 / 64	04A0000-04BFFFF	0250000-025FFFF
38	128 / 64	04C0000-04DFFFF	0260000-026FFFF
39	128 / 64	04E0000-04FFFFF	0270000-027FFFF
40	128 / 64	0500000-051FFFF	0280000-028FFFF
41	128 / 64	0520000-053FFFF	0290000-029FFFF
42	128 / 64	0540000-055FFFF	02A0000-02AFFFF
43	128 / 64	0560000-057FFFF	02B0000-02BFFFF
44	128 / 64	0580000-059FFFF	02C0000-02CFFFF
45	128 / 64	05A0000-05BFFFF	02D0000-02DFFFF
46	128 / 64	05C0000-05DFFFF	02E0000-02EFFFF
47	128 / 64	05E0000-05FFFFF	02F0000-02FFFFF
48	128 / 64	0600000-061FFFF	0300000-030FFFF
49	128 / 64	0620000-063FFFF	0310000-031FFFF
50	128 / 64	0640000-065FFFF	0320000-032FFFF
51	128 / 64	0660000-067FFFF	0330000-033FFFF
52	128 / 64	0680000-069FFFF	0340000-034FFFF
53	128 / 64	06A0000-06BFFFF	0350000-035FFFF
54	128 / 64	06C0000-06DFFFF	0360000-036FFFF
55	128 / 64	06E0000-06FFFFF	0370000-037FFFF
56	128 / 64	0700000-071FFFF	0380000-038FFFF
57	128 / 64	0720000-073FFFF	0390000-039FFFF
58	128 / 64	0740000-075FFFF	03A0000-03AFFFF
59	128 / 64	0760000-077FFFF	03B0000-03BFFFF
60	128 / 64	0780000-079FFFF	03C0000-03CFFFF
61	128 / 64	07A0000-07BFFFF	03D0000-03DFFFF
62	128 / 64	07C0000-07DFFFF	03E0000-03EFFFF
63	128 / 64	07E0000-07FFFFF	03F0000-03FFFFF
64	128 / 64	0800000-081FFFF	0400000-040FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
65	128 / 64	0820000-083FFFF	0410000-041FFFF
66	128 / 64	0840000-085FFFF	0420000-042FFFF
67	128 / 64	0860000-087FFFF	0430000-043FFFF
68	128 / 64	0880000-089FFFF	0440000-044FFFF
69	128 / 64	08A0000-08BFFFF	0450000-045FFFF
70	128 / 64	08C0000-08DFFFF	0460000-046FFFF
71	128 / 64	08E0000-08FFFFF	0470000-047FFFF
72	128 / 64	0900000-091FFFF	0480000-048FFFF
73	128 / 64	0920000-093FFFF	0490000-049FFFF
74	128 / 64	0940000-095FFFF	04A0000-04AFFFF
75	128 / 64	0960000-097FFFF	04B0000-04BFFFF
76	128 / 64	0980000-099FFFF	04C0000-04CFFFF
77	128 / 64	09A0000-09BFFFF	04D0000-04DFFFF
78	128 / 64	09C0000-09DFFFF	04E0000-04EFFFF
79	128 / 64	09E0000-09FFFFF	04F0000-04FFFFF
80	128 / 64	0A00000-0A1FFFF	0500000-050FFFF
81	128 / 64	0A20000-0A3FFFF	0510000-051FFFF
82	128 / 64	0A40000-0A5FFFF	0520000-052FFFF
83	128 / 64	0A60000-0A7FFFF	0530000-053FFFF
84	128 / 64	0A80000-0A9FFFF	0540000-054FFFF
85	128 / 64	0AA0000-0ABFFFF	0550000-055FFFF
86	128 / 64	0AC0000-0ADFFFF	0560000-056FFFF
87	128 / 64	0AE0000-0AFFFFF	0570000-057FFFF
88	128 / 64	0B00000-0B1FFFF	0580000-058FFFF
89	128 / 64	0B20000-0B3FFFF	0590000-059FFFF
90	128 / 64	0B40000-0B5FFFF	05A0000-05AFFFF
91	128 / 64	0B60000-0B7FFFF	05B0000-05BFFFF
92	128 / 64	0B80000-0B9FFFF	05C0000-05CFFFF
93	128 / 64	0BA0000-0BBFFFF	05D0000-05DFFFF
94	128 / 64	0BC0000-0BDFFFF	05E0000-05EFFFF
95	128 / 64	0BE0000-0BFFFFF	05F0000-05FFFFF
96	128 / 64	0C00000-0C1FFFF	0600000-060FFFF
97	128 / 64	0C20000-0C3FFFF	0610000-061FFFF
98	128 / 64	0C40000-0C5FFFF	0620000-062FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
99	128 / 64	0C60000-0C7FFFF	0630000-063FFFF
100	128 / 64	0C80000-0C9FFFF	0640000-064FFFF
101	128 / 64	0CA0000-0CBFFFF	0650000-065FFFF
102	128 / 64	0CC0000-0CDFFFF	0660000-066FFFF
103	128 / 64	0CE0000-0CFFFFF	0670000-067FFFF
104	128 / 64	0D00000-0D1FFFF	0680000-068FFFF
105	128 / 64	0D20000-0D3FFFF	0690000-069FFFF
106	128 / 64	0D40000-0D5FFFF	06A0000-06AFFFF
107	128 / 64	0D60000-0D7FFFF	06B0000-06BFFFF
108	128 / 64	0D80000-0D9FFFF	06C0000-06CFFFF
109	128 / 64	0DA0000-0DBFFFF	06D0000-06DFFFF
110	128 / 64	0DC0000-0DDFFFF	06E0000-06EFFFF
111	128 / 64	0DE0000-0DFFFFF	06F0000-06FFFFF
112	128 / 64	0E00000-0E1FFFF	0700000-070FFFF
113	128 / 64	0E20000-0E3FFFF	0710000-071FFFF
114	128 / 64	0E40000-0E5FFFF	0720000-072FFFF
115	128 / 64	0E60000-0E7FFFF	0730000-073FFFF
116	128 / 64	0E80000-0E9FFFF	0740000-074FFFF
117	128 / 64	0EA0000-0EBFFFF	0750000-075FFFF
118	128 / 64	0EC0000-0EDFFFF	0760000-076FFFF
119	128 / 64	0EE0000-0EFFFFF	0770000-077FFFF
120	128 / 64	0F00000-0F1FFFF	0780000-078FFFF
121	128 / 64	0F20000-0F3FFFF	0790000-079FFFF
122	128 / 64	0F40000-0F5FFFF	07A0000-07AFFFF
123	128 / 64	0F60000-0F7FFFF	07B0000-07BFFFF
124	128 / 64	0F80000-0F9FFFF	07C0000-07CFFFF
125	128 / 64	0FA0000-0FBFFFF	07D0000-07DFFFF
126	128 / 64	0FC0000-0FDFFFF	07E0000-07EFFFF
127	128 / 64	0FE0000-0FFFFFF	07F0000-07FFFFF
128	128 / 64	1000000-101FFFF	0800000-080FFFF
129	128 / 64	1020000-103FFFF	0810000-081FFFF
130	128 / 64	1040000-105FFFF	0820000-082FFFF
131	128 / 64	1060000-107FFFF	0830000-083FFFF
132	128 / 64	1080000-109FFFF	0840000-084FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
133	128 / 64	10A0000-10BFFFF	0850000-085FFFF
134	128 / 64	10C0000-10DFFFF	0860000-086FFFF
135	128 / 64	10E0000-10FFFFF	0870000-087FFFF
136	128 / 64	1100000-111FFFF	0880000-088FFFF
137	128 / 64	1120000-113FFFF	0890000-089FFFF
138	128 / 64	1140000-115FFFF	08A0000-08AFFFF
139	128 / 64	1160000-117FFFF	08B0000-08BFFFF
140	128 / 64	1180000-119FFFF	08C0000-08CFFFF
141	128 / 64	11A0000-11BFFFF	08D0000-08DFFFF
142	128 / 64	11C0000-11DFFFF	08E0000-08EFFFF
143	128 / 64	11E0000-11FFFFF	08F0000-08FFFFF
144	128 / 64	1200000-121FFFF	0900000-090FFFF
145	128 / 64	1220000-123FFFF	0910000-091FFFF
146	128 / 64	1240000-125FFFF	0920000-092FFFF
147	128 / 64	1260000-127FFFF	0930000-093FFFF
148	128 / 64	1280000-129FFFF	0940000-094FFFF
149	128 / 64	12A0000-12BFFFF	0950000-095FFFF
150	128 / 64	12C0000-12DFFFF	0960000-096FFFF
151	128 / 64	12E0000-12FFFFF	0970000-097FFFF
152	128 / 64	1300000-131FFFF	0980000-098FFFF
153	128 / 64	1320000-133FFFF	0990000-099FFFF
154	128 / 64	1340000-135FFFF	09A0000-09AFFFF
155	128 / 64	1360000-137FFFF	09B0000-09BFFFF
156	128 / 64	1380000-139FFFF	09C0000-09CFFFF
157	128 / 64	13A0000-13BFFFF	09D0000-09DFFFF
158	128 / 64	13C0000-13DFFFF	09E0000-09EFFFF
159	128 / 64	13E0000-13FFFFF	09F0000-09FFFFF
160	128 / 64	1400000-141FFFF	0A00000-0A0FFFF
161	128 / 64	1420000-143FFFF	0A10000-0A1FFFF
162	128 / 64	1440000-145FFFF	0A20000-0A2FFFF
163	128 / 64	1460000-147FFFF	0A30000-0A3FFFF
164	128 / 64	1480000-149FFFF	0A40000-0A4FFFF
165	128 / 64	14A0000-14BFFFF	0A50000-0A5FFFF
166	128 / 64	14C0000-14DFFFF	0A60000-0A6FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
167	128 / 64	14E0000-14FFFFF	0A70000-0A7FFFF
168	128 / 64	1500000-151FFFF	0A80000-0A8FFFF
169	128 / 64	1520000-153FFFF	0A90000-0A9FFFF
170	128 / 64	1540000-155FFFF	0AA0000-0AAFFFF
171	128 / 64	1560000-157FFFF	0AB0000-0ABFFFF
172	128 / 64	1580000-159FFFF	0AC0000-0ACFFFF
173	128 / 64	15A0000-15BFFFF	0AD0000-0ADFFFF
174	128 / 64	15C0000-15DFFFF	0AE0000-0AEFFFF
175	128 / 64	15E0000-15FFFFF	0AF0000-0AFFFFF
176	128 / 64	1600000-161FFFF	0B00000-0B0FFFF
177	128 / 64	1620000-163FFFF	0B10000-0B1FFFF
178	128 / 64	1640000-165FFFF	0B20000-0B2FFFF
179	128 / 64	1660000-167FFFF	0B30000-0B3FFFF
180	128 / 64	1680000-169FFFF	0B40000-0B4FFFF
181	128 / 64	16A0000-16BFFFF	0B50000-0B5FFFF
182	128 / 64	16C0000-16DFFFF	0B60000-0B6FFFF
183	128 / 64	16E0000-16FFFFF	0B70000-0B7FFFF
184	128 / 64	1700000-171FFFF	0B80000-0B8FFFF
185	128 / 64	1720000-173FFFF	0B90000-0B9FFFF
186	128 / 64	1740000-175FFFF	0BA0000-0BAFFFF
187	128 / 64	1760000-177FFFF	0BB0000-0BBFFFF
188	128 / 64	1780000-179FFFF	0BC0000-0BCFFFF
189	128 / 64	17A0000-17BFFFF	0BD0000-0BDFFFF
190	128 / 64	17C0000-17DFFFF	0BE0000-0BEFFFF
191	128 / 64	17E0000-17FFFFF	0BF0000-0BFFFFF
192	128 / 64	1800000-181FFFF	0C00000-0C0FFFF
193	128 / 64	1820000-183FFFF	0C10000-0C1FFFF
194	128 / 64	1840000-185FFFF	0C20000-0C2FFFF
195	128 / 64	1860000-187FFFF	0C30000-0C3FFFF
196	128 / 64	1880000-189FFFF	0C40000-0C4FFFF
197	128 / 64	18A0000-18BFFFF	0C50000-0C5FFFF
198	128 / 64	18C0000-18DFFFF	0C60000-0C6FFFF
199	128 / 64	18E0000-18FFFFF	0C70000-0C7FFFF
200	128 / 64	1900000-191FFFF	0C80000-0C8FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
201	128 / 64	1920000-193FFFF	0C90000-0C9FFFF
202	128 / 64	1940000-195FFFF	0CA0000-0CAFFFF
203	128 / 64	1960000-197FFFF	0CB0000-0CBFFFF
204	128 / 64	1980000-199FFFF	0CC0000-0CCFFFF
205	128 / 64	19A0000-19BFFFF	0CD0000-0CDFFFF
206	128 / 64	19C0000-19DFFFF	0CE0000-0CEFFFF
207	128 / 64	19E0000-19FFFFF	0CF0000-0CFFFFF
208	128 / 64	1A00000-1A1FFFF	0D00000-0D0FFFF
209	128 / 64	1A20000-1A3FFFF	0D10000-0D1FFFF
210	128 / 64	1A40000-1A5FFFF	0D20000-0D2FFFF
211	128 / 64	1A60000-1A7FFFF	0D30000-0D3FFFF
212	128 / 64	1A80000-1A9FFFF	0D40000-0D4FFFF
213	128 / 64	1AA0000-1ABFFFF	0D50000-0D5FFFF
214	128 / 64	1AC0000-1ADFFFF	0D60000-0D6FFFF
215	128 / 64	1AE0000-1AFFFFF	0D70000-0D7FFFF
216	128 / 64	1B00000-1B1FFFF	0D80000-0D8FFFF
217	128 / 64	1B20000-1B3FFFF	0D90000-0D9FFFF
218	128 / 64	1B40000-1B5FFFF	0DA0000-0DAFFFF
219	128 / 64	1B60000-1B7FFFF	0DB0000-0DBFFFF
220	128 / 64	1B80000-1B9FFFF	0DC0000-0DCFFFF
221	128 / 64	1BA0000-1BBFFFF	0DD0000-0DDFFFF
222	128 / 64	1BC0000-1BDFFFF	0DE0000-0DEFFFF
223	128 / 64	1BE0000-1BFFFFF	0DF0000-0DFFFFF
224	128 / 64	1C00000-1C1FFFF	0E00000-0E0FFFF
225	128 / 64	1C20000-1C3FFFF	0E10000-0E1FFFF
226	128 / 64	1C40000-1C5FFFF	0E20000-0E2FFFF
227	128 / 64	1C60000-1C7FFFF	0E30000-0E3FFFF
228	128 / 64	1C80000-1C9FFFF	0E40000-0E4FFFF
229	128 / 64	1CA0000-1CBFFFF	0E50000-0E5FFFF
230	128 / 64	1CC0000-1CDFFFF	0E60000-0E6FFFF
231	128 / 64	1CE0000-1CFFFFF	0E70000-0E7FFFF
232	128 / 64	1D00000-1D1FFFF	0E80000-0E8FFFF
233	128 / 64	1D20000-1D3FFFF	0E90000-0E9FFFF
234	128 / 64	1D40000-1D5FFFF	0EA0000-0EAFFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
235	128 / 64	1D60000-1D7FFFF	0EB0000-0EBFFFF
236	128 / 64	1D80000-1D9FFFF	0EC0000-0ECFFFF
237	128 / 64	1DA0000-1DBFFFF	0ED0000-0EDFFFF
238	128 / 64	1DC0000-1DDFFFF	0EE0000-0EEFFFF
239	128 / 64	1DE0000-1DFFFFF	0EF0000-0EFFFFF
240	128 / 64	1E00000-1E1FFFF	0F00000-0F0FFFF
241	128 / 64	1E20000-1E3FFFF	0F10000-0F1FFFF
242	128 / 64	1E40000-1E5FFFF	0F20000-0F2FFFF
243	128 / 64	1E60000-1E7FFFF	0F30000-0F3FFFF
244	128 / 64	1E80000-1E9FFFF	0F40000-0F4FFFF
245	128 / 64	1EA0000-1EBFFFF	0F50000-0F5FFFF
246	128 / 64	1EC0000-1EDFFFF	0F60000-0F6FFFF
247	128 / 64	1EE0000-1EFFFFF	0F70000-0F7FFFF
248	128 / 64	1F00000-1F1FFFF	0F80000-0F8FFFF
249	128 / 64	1F20000-1F3FFFF	0F90000-0F9FFFF
250	128 / 64	1F40000-1F5FFFF	0FA0000-0FAFFFF
251	128 / 64	1F60000-1F7FFFF	0FB0000-0FBFFFF
252	128 / 64	1F80000-1F9FFFF	0FC0000-0FCFFFF
253	128 / 64	1FA0000-1FBFFFF	0FD0000-0FDFFFF
254	128 / 64	1FC0000-1FDFFFF	0FE0000-0FEFFFF
255	128 / 64	1FE0000-1FFFFFF	0FF0000-0FFFFFF
256	128 / 64	2000000-201FFFF	1000000-100FFFF
257	128 / 64	2020000-203FFFF	1010000-101FFFF
258	128 / 64	2040000-205FFFF	1020000-102FFFF
259	128 / 64	2060000-207FFFF	1030000-103FFFF
260	128 / 64	2080000-209FFFF	1040000-104FFFF
261	128 / 64	20A0000-20BFFFF	1050000-105FFFF
262	128 / 64	20C0000-20DFFFF	1060000-106FFFF
263	128 / 64	20E0000-20FFFFF	1070000-107FFFF
264	128 / 64	2100000-211FFFF	1080000-108FFFF
265	128 / 64	2120000-213FFFF	1090000-109FFFF
266	128 / 64	2140000-215FFFF	10A0000-10AFFFF
267	128 / 64	2160000-217FFFF	10B0000-10BFFFF
268	128 / 64	2180000-219FFFF	10C0000-10CFFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
269	128 / 64	21A0000-21BFFFF	10D0000-10DFFFF
270	128 / 64	21C0000-21DFFFF	10E0000-10EFFFF
271	128 / 64	21E0000-21FFFFF	10F0000-10FFFFF
272	128 / 64	2200000-221FFFF	1100000-110FFFF
273	128 / 64	2220000-223FFFF	1110000-111FFFF
274	128 / 64	2240000-225FFFF	1120000-112FFFF
275	128 / 64	2260000-227FFFF	1130000-113FFFF
276	128 / 64	2280000-229FFFF	1140000-114FFFF
277	128 / 64	22A0000-22BFFFF	1150000-115FFFF
278	128 / 64	22C0000-22DFFFF	1160000-116FFFF
279	128 / 64	22E0000-22FFFFF	1170000-117FFFF
280	128 / 64	2300000-231FFFF	1180000-118FFFF
281	128 / 64	2320000-233FFFF	1190000-119FFFF
282	128 / 64	2340000-235FFFF	11A0000-11AFFFF
283	128 / 64	2360000-237FFFF	11B0000-11BFFFF
284	128 / 64	2380000-239FFFF	11C0000-11CFFFF
285	128 / 64	23A0000-23BFFFF	11D0000-11DFFFF
286	128 / 64	23C0000-23DFFFF	11E0000-11EFFFF
287	128 / 64	23E0000-23FFFFF	11F0000-11FFFFF
288	128 / 64	2400000-241FFFF	1200000-120FFFF
289	128 / 64	2420000-243FFFF	1210000-121FFFF
290	128 / 64	2440000-245FFFF	1220000-122FFFF
291	128 / 64	2460000-247FFFF	1230000-123FFFF
292	128 / 64	2480000-249FFFF	1240000-124FFFF
293	128 / 64	24A0000-24BFFFF	1250000-125FFFF
294	128 / 64	24C0000-24DFFFF	1260000-126FFFF
295	128 / 64	24E0000-24FFFFF	1270000-127FFFF
296	128 / 64	2500000-251FFFF	1280000-128FFFF
297	128 / 64	2520000-253FFFF	1290000-129FFFF
298	128 / 64	2540000-255FFFF	12A0000-12AFFFF
299	128 / 64	2560000-257FFFF	12B0000-12BFFFF
300	128 / 64	2580000-259FFFF	12C0000-12CFFFF
301	128 / 64	25A0000-25BFFFF	12D0000-12DFFFF
302	128 / 64	25C0000-25DFFFF	12E0000-12EFFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
303	128 / 64	25E0000-25FFFFF	12F0000-12FFFFF
304	128 / 64	2600000-261FFFF	1300000-130FFFF
305	128 / 64	2620000-263FFFF	1310000-131FFFF
306	128 / 64	2640000-265FFFF	1320000-132FFFF
307	128 / 64	2660000-267FFFF	1330000-133FFFF
308	128 / 64	2680000-269FFFF	1340000-134FFFF
309	128 / 64	26A0000-26BFFFF	1350000-135FFFF
310	128 / 64	26C0000-26DFFFF	1360000-136FFFF
311	128 / 64	26E0000-26FFFFF	1370000-137FFFF
312	128 / 64	2700000-271FFFF	1380000-138FFFF
313	128 / 64	2720000-273FFFF	1390000-139FFFF
314	128 / 64	2740000-275FFFF	13A0000-13AFFFF
315	128 / 64	2760000-277FFFF	13B0000-13BFFFF
316	128 / 64	2780000-279FFFF	13C0000-13CFFFF
317	128 / 64	27A0000-27BFFFF	13D0000-13DFFFF
318	128 / 64	27C0000-27DFFFF	13E0000-13EFFFF
319	128 / 64	27E0000-27FFFFF	13F0000-13FFFFF
320	128 / 64	2800000-281FFFF	1400000-140FFFF
321	128 / 64	2820000-283FFFF	1410000-141FFFF
322	128 / 64	2840000-285FFFF	1420000-142FFFF
323	128 / 64	2860000-287FFFF	1430000-143FFFF
324	128 / 64	2880000-289FFFF	1440000-144FFFF
325	128 / 64	28A0000-28BFFFF	1450000-145FFFF
326	128 / 64	28C0000-28DFFFF	1460000-146FFFF
327	128 / 64	28E0000-28FFFFF	1470000-147FFFF
328	128 / 64	2900000-291FFFF	1480000-148FFFF
329	128 / 64	2920000-293FFFF	1490000-149FFFF
330	128 / 64	2940000-295FFFF	14A0000-14AFFFF
331	128 / 64	2960000-297FFFF	14B0000-14BFFFF
332	128 / 64	2980000-299FFFF	14C0000-14CFFFF
333	128 / 64	29A0000-29BFFFF	14D0000-14DFFFF
334	128 / 64	29C0000-29DFFFF	14E0000-14EFFFF
335	128 / 64	29E0000-29FFFFF	14F0000-14FFFFF
336	128 / 64	2A00000-2A1FFFF	1500000-150FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
337	128 / 64	2A20000-2A3FFFF	1510000-151FFFF
338	128 / 64	2A40000-2A5FFFF	1520000-152FFFF
339	128 / 64	2A60000-2A7FFFF	1530000-153FFFF
340	128 / 64	2A80000-2A9FFFF	1540000-154FFFF
341	128 / 64	2AA0000-2ABFFFF	1550000-155FFFF
342	128 / 64	2AC0000-2ADFFFF	1560000-156FFFF
343	128 / 64	2AE0000-2AFFFFF	1570000-157FFFF
344	128 / 64	2B00000-2B1FFFF	1580000-158FFFF
345	128 / 64	2B20000-2B3FFFF	1590000-159FFFF
346	128 / 64	2B40000-2B5FFFF	15A0000-15AFFFF
347	128 / 64	2B60000-2B7FFFF	15B0000-15BFFFF
348	128 / 64	2B80000-2B9FFFF	15C0000-15CFFFF
349	128 / 64	2BA0000-2BBFFFF	15D0000-15DFFFF
350	128 / 64	2BC0000-2BDFFFF	15E0000-15EFFFF
351	128 / 64	2BE0000-2BFFFFF	15F0000-15FFFFF
352	128 / 64	2C00000-2C1FFFF	1600000-160FFFF
353	128 / 64	2C20000-2C3FFFF	1610000-161FFFF
354	128 / 64	2C40000-2C5FFFF	1620000-162FFFF
355	128 / 64	2C60000-2C7FFFF	1630000-163FFFF
356	128 / 64	2C80000-2C9FFFF	1640000-164FFFF
357	128 / 64	2CA0000-2CBFFFF	1650000-165FFFF
358	128 / 64	2CC0000-2CDFFFF	1660000-166FFFF
359	128 / 64	2CE0000-2CFFFFF	1670000-167FFFF
360	128 / 64	2D00000-2D1FFFF	1680000-068FFFF
361	128 / 64	2D20000-2D3FFFF	1690000-169FFFF
362	128 / 64	2D40000-2D5FFFF	16A0000-16AFFFF
363	128 / 64	2D60000-2D7FFFF	16B0000-16BFFFF
364	128 / 64	2D80000-2D9FFFF	16C0000-16CFFFF
365	128 / 64	2DA0000-2DBFFFF	16D0000-16DFFFF
366	128 / 64	2DC0000-2DDFFFF	16E0000-16EFFFF
367	128 / 64	2DE0000-2DFFFFF	16F0000-16FFFFF
368	128 / 64	2E00000-2E1FFFF	1700000-170FFFF
369	128 / 64	2E20000-2E3FFFF	1710000-171FFFF
370	128 / 64	2E40000-2E5FFFF	1720000-172FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
371	128 / 64	2E60000-2E7FFFF	1730000-173FFFF
372	128 / 64	2E80000-2E9FFFF	1740000-174FFFF
373	128 / 64	2EA0000-2EBFFFF	1750000-175FFFF
374	128 / 64	2EC0000-2EDFFFF	1760000-176FFFF
375	128 / 64	2EE0000-2EFFFFF	1770000-177FFFF
376	128 / 64	2F00000-2F1FFFF	1780000-178FFFF
377	128 / 64	2F20000-2F3FFFF	1790000-179FFFF
378	128 / 64	2F40000-2F5FFFF	17A0000-17AFFFF
379	128 / 64	2F60000-2F7FFFF	17B0000-17BFFFF
380	128 / 64	2F80000-2F9FFFF	17C0000-17CFFFF
381	128 / 64	2FA0000-2FBFFFF	17D0000-17DFFFF
382	128 / 64	2FC0000-2FDFFFF	17E0000-17EFFFF
383	128 / 64	2FE0000-2FFFFFF	17F0000-17FFFFF
384	128 / 64	3000000-301FFFF	1800000-180FFFF
385	128 / 64	3020000-303FFFF	1810000-181FFFF
386	128 / 64	3040000-305FFFF	1820000-182FFFF
387	128 / 64	3060000-307FFFF	1830000-183FFFF
388	128 / 64	3080000-309FFFF	1840000-184FFFF
389	128 / 64	30A0000-30BFFFF	1850000-185FFFF
390	128 / 64	30C0000-30DFFFF	1860000-186FFFF
391	128 / 64	30E0000-30FFFFF	1870000-187FFFF
392	128 / 64	3100000-311FFFF	1880000-188FFFF
393	128 / 64	3120000-313FFFF	1890000-189FFFF
394	128 / 64	3140000-315FFFF	18A0000-18AFFFF
395	128 / 64	3160000-317FFFF	18B0000-18BFFFF
396	128 / 64	3180000-319FFFF	18C0000-18CFFFF
397	128 / 64	31A0000-31BFFFF	18D0000-18DFFFF
398	128 / 64	31C0000-31DFFFF	18E0000-18EFFFF
399	128 / 64	31E0000-31FFFFF	18F0000-18FFFFF
400	128 / 64	3200000-321FFFF	1900000-190FFFF
401	128 / 64	3220000-323FFFF	1910000-191FFFF
402	128 / 64	3240000-325FFFF	1920000-192FFFF
403	128 / 64	3260000-327FFFF	1930000-193FFFF
404	128 / 64	3280000-329FFFF	1940000-194FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
405	128 / 64	32A0000-32BFFFF	1950000-195FFFF
406	128 / 64	32C0000-32DFFFF	1960000-196FFFF
407	128 / 64	32E0000-32FFFFF	1970000-197FFFF
408	128 / 64	3300000-331FFFF	1980000-198FFFF
409	128 / 64	3320000-333FFFF	1990000-199FFFF
410	128 / 64	3340000-335FFFF	19A0000-19AFFFF
411	128 / 64	3360000-337FFFF	19B0000-19BFFFF
412	128 / 64	3380000-339FFFF	19C0000-19CFFFF
413	128 / 64	33A0000-33BFFFF	19D0000-19DFFFF
414	128 / 64	33C0000-33DFFFF	19E0000-19EFFFF
415	128 / 64	33E0000-33FFFFF	19F0000-19FFFFF
416	128 / 64	3400000-341FFFF	1A00000-1A0FFFF
417	128 / 64	3420000-343FFFF	1A10000-1A1FFFF
418	128 / 64	3440000-345FFFF	1A20000-1A2FFFF
419	128 / 64	3460000-347FFFF	1A30000-1A3FFFF
420	128 / 64	3480000-349FFFF	1A40000-1A4FFFF
421	128 / 64	34A0000-34BFFFF	1A50000-1A5FFFF
422	128 / 64	34C0000-34DFFFF	1A60000-1A6FFFF
423	128 / 64	34E0000-34FFFFF	1A70000-1A7FFFF
424	128 / 64	3500000-351FFFF	1A80000-1A8FFFF
425	128 / 64	3520000-353FFFF	1A90000-1A9FFFF
426	128 / 64	3540000-355FFFF	1AA0000-1AAFFFF
427	128 / 64	3560000-357FFFF	1AB0000-1ABFFFF
428	128 / 64	3580000-359FFFF	1AC0000-1ACFFFF
429	128 / 64	35A0000-35BFFFF	1AD0000-1ADFFFF
430	128 / 64	35C0000-35DFFFF	1AE0000-1AEFFFF
431	128 / 64	35E0000-35FFFFF	1AF0000-1AFFFFF
432	128 / 64	3600000-361FFFF	1B00000-1B0FFFF
433	128 / 64	3620000-363FFFF	1B10000-1B1FFFF
434	128 / 64	3640000-365FFFF	1B20000-1B2FFFF
435	128 / 64	3660000-367FFFF	1B30000-1B3FFFF
436	128 / 64	3680000-369FFFF	1B40000-1B4FFFF
437	128 / 64	36A0000-36BFFFF	1B50000-1B5FFFF
438	128 / 64	36C0000-36DFFFF	1B60000-1B6FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
439	128 / 64	36E0000-36FFFFF	1B70000-1B7FFFF
440	128 / 64	3700000-371FFFF	1B80000-1B8FFFF
441	128 / 64	3720000-373FFFF	1B90000-1B9FFFF
442	128 / 64	3740000-375FFFF	1BA0000-1BAFFFF
443	128 / 64	3760000-377FFFF	1BB0000-1BBFFFF
444	128 / 64	3780000-379FFFF	1BC0000-1BCFFFF
445	128 / 64	37A0000-37BFFFF	1BD0000-1BDFFFF
446	128 / 64	37C0000-37DFFFF	1BE0000-1BEFFFF
447	128 / 64	37E0000-37FFFFF	1BF0000-1BFFFFF
448	128 / 64	3800000-381FFFF	1C00000-1C0FFFF
449	128 / 64	3820000-383FFFF	1C10000-1C1FFFF
450	128 / 64	3840000-385FFFF	1C20000-1C2FFFF
451	128 / 64	3860000-387FFFF	1C30000-1C3FFFF
452	128 / 64	3880000-389FFFF	1C40000-1C4FFFF
453	128 / 64	38A0000-38BFFFF	1C50000-1C5FFFF
454	128 / 64	38C0000-38DFFFF	1C60000-1C6FFFF
455	128 / 64	38E0000-38FFFFF	1C70000-1C7FFFF
456	128 / 64	3900000-391FFFF	1C80000-1C8FFFF
457	128 / 64	3920000-393FFFF	1C90000-1C9FFFF
458	128 / 64	3940000-395FFFF	1CA0000-1CAFFFF
459	128 / 64	3960000-397FFFF	1CB0000-1CBFFFF
460	128 / 64	3980000-399FFFF	1CC0000-1CCFFFF
461	128 / 64	39A0000-39BFFFF	1CD0000-1CDFFFF
462	128 / 64	39C0000-39DFFFF	1CE0000-1CEFFFF
463	128 / 64	39E0000-39FFFFF	1CF0000-1CFFFFF
464	128 / 64	3A00000-3A1FFFF	1D00000-1D0FFFF
465	128 / 64	3A20000-3A3FFFF	1D10000-1D1FFFF
466	128 / 64	3A40000-3A5FFFF	1D20000-1D2FFFF
467	128 / 64	3A60000-3A7FFFF	1D30000-1D3FFFF
468	128 / 64	3A80000-3A9FFFF	1D40000-1D4FFFF
469	128 / 64	3AA0000-3ABFFFF	1D50000-1D5FFFF
470	128 / 64	3AC0000-3ADFFFF	1D60000-1D6FFFF
471	128 / 64	3AE0000-3AFFFFF	1D70000-1D7FFFF
472	128 / 64	3B00000-3B1FFFF	1D80000-1D8FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
473	128 / 64	3B20000-3B3FFFF	1D90000-1D9FFFF
474	128 / 64	3B40000-3B5FFFF	1DA0000-1DAFFFF
475	128 / 64	3B60000-3B7FFFF	1DB0000-1DBFFFF
476	128 / 64	3B80000-3B9FFFF	1DC0000-1DCFFFF
477	128 / 64	3BA0000-3BBFFFF	1DD0000-1DDFFFF
478	128 / 64	3BC0000-3BDFFFF	1DE0000-1DEFFFF
479	128 / 64	3BE0000-3BFFFFF	1DF0000-1DFFFFF
480	128 / 64	3C00000-3C1FFFF	1E00000-1E0FFFF
481	128 / 64	3C20000-3C3FFFF	1E10000-1E1FFFF
482	128 / 64	3C40000-3C5FFFF	1E20000-1E2FFFF
483	128 / 64	3C60000-3C7FFFF	1E30000-1E3FFFF
484	128 / 64	3C80000-3C9FFFF	1E40000-1E4FFFF
485	128 / 64	3CA0000-3CBFFFF	1E50000-1E5FFFF
486	128 / 64	3CC0000-3CDFFFF	1E60000-1E6FFFF
487	128 / 64	3CE0000-3CFFFFF	1E70000-1E7FFFF
488	128 / 64	3D00000-3D1FFFF	1E80000-1E8FFFF
489	128 / 64	3D20000-3D3FFFF	1E90000-1E9FFFF
490	128 / 64	3D40000-3D5FFFF	1EA0000-1EAFFFF
491	128 / 64	3D60000-3D7FFFF	1EB0000-1EBFFFF
492	128 / 64	3D80000-3D9FFFF	1EC0000-1ECFFFF
493	128 / 64	3DA0000-3DBFFFF	1ED0000-1EDFFFF
494	128 / 64	3DC0000-3DDFFFF	1EE0000-1EEFFFF
495	128 / 64	3DE0000-3DFFFFF	1EF0000-1EFFFFF
496	128 / 64	3E00000-3E1FFFF	1F00000-1F0FFFF
497	128 / 64	3E20000-3E3FFFF	1F10000-1F1FFFF
498	128 / 64	3E40000-3E5FFFF	1F20000-1F2FFFF
499	128 / 64	3E60000-3E7FFFF	1F30000-1F3FFFF
500	128 / 64	3E80000-3E9FFFF	1F40000-1F4FFFF
501	128 / 64	3EA0000-3EBFFFF	1F50000-1F5FFFF
502	128 / 64	3EC0000-3EDFFFF	1F60000-1F6FFFF
503	128 / 64	3EE0000-3EFFFFF	1F70000-1F7FFFF
504	128 / 64	3F00000-3F1FFFF	1F80000-1F8FFFF
505	128 / 64	3F20000-3F3FFFF	1F90000-1F9FFFF
506	128 / 64	3F40000-3F5FFFF	1FA0000-1FAFFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
507	128 / 64	3F60000-3F7FFFF	1FB0000-1FBFFFF
508	128 / 64	3F80000-3F9FFFF	1FC0000-1FCFFFF
509	128 / 64	3FA0000-3FBFFFF	1FD0000-1FDFFFF
510	128 / 64	3FC0000-3FDFFFF	1FE0000-1FEFFFF
511	128 / 64	3FE0000-3FFFFFF	1FF0000-1FFFFFF
512	128 / 64	4000000-401FFFF	2000000-200FFFF
513	128 / 64	4020000-403FFFF	2010000-201FFFF
514	128 / 64	4040000-405FFFF	2020000-202FFFF
515	128 / 64	4060000-407FFFF	2030000-203FFFF
516	128 / 64	4080000-409FFFF	2040000-204FFFF
517	128 / 64	40A0000-40BFFFF	2050000-205FFFF
518	128 / 64	40C0000-40DFFFF	2060000-206FFFF
519	128 / 64	40E0000-40FFFFF	2070000-207FFFF
520	128 / 64	4100000-411FFFF	2080000-208FFFF
521	128 / 64	4120000-413FFFF	2090000-209FFFF
522	128 / 64	4140000-415FFFF	20A0000-20AFFFF
523	128 / 64	4160000-417FFFF	20B0000-20BFFFF
524	128 / 64	4180000-419FFFF	20C0000-20CFFFF
525	128 / 64	41A0000-41BFFFF	20D0000-20DFFFF
526	128 / 64	41C0000-41DFFFF	20E0000-20EFFFF
527	128 / 64	41E0000-41FFFFF	20F0000-20FFFFF
528	128 / 64	4200000-421FFFF	2100000-210FFFF
529	128 / 64	4220000-423FFFF	2110000-211FFFF
530	128 / 64	4240000-425FFFF	2120000-212FFFF
531	128 / 64	4260000-427FFFF	2130000-213FFFF
532	128 / 64	4280000-429FFFF	2140000-214FFFF
533	128 / 64	42A0000-42BFFFF	2150000-215FFFF
534	128 / 64	42C0000-42DFFFF	2160000-216FFFF
535	128 / 64	42E0000-42FFFFF	2170000-217FFFF
536	128 / 64	4300000-431FFFF	2180000-218FFFF
537	128 / 64	4320000-433FFFF	2190000-219FFFF
538	128 / 64	4340000-435FFFF	21A0000-21AFFFF
539	128 / 64	4360000-437FFFF	21B0000-21BFFFF
540	128 / 64	4380000-439FFFF	21C0000-21CFFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
541	128 / 64	43A0000-43BFFFF	21D0000-21DFFFF
542	128 / 64	43C0000-43DFFFF	21E0000-21EFFFF
543	128 / 64	43E0000-43FFFFF	21F0000-21FFFFF
544	128 / 64	4400000-441FFFF	2200000-220FFFF
545	128 / 64	4420000-443FFFF	2210000-221FFFF
546	128 / 64	4440000-445FFFF	2220000-222FFFF
547	128 / 64	4460000-447FFFF	2230000-223FFFF
548	128 / 64	4480000-449FFFF	2240000-224FFFF
549	128 / 64	44A0000-44BFFFF	2250000-225FFFF
550	128 / 64	44C0000-44DFFFF	2260000-226FFFF
551	128 / 64	44E0000-44FFFFF	2270000-227FFFF
552	128 / 64	4500000-451FFFF	2280000-228FFFF
553	128 / 64	4520000-453FFFF	2290000-229FFFF
554	128 / 64	4540000-455FFFF	22A0000-22AFFFF
555	128 / 64	4560000-457FFFF	22B0000-22BFFFF
556	128 / 64	4580000-459FFFF	22C0000-22CFFFF
557	128 / 64	45A0000-45BFFFF	22D0000-22DFFFF
558	128 / 64	45C0000-45DFFFF	22E0000-22EFFFF
559	128 / 64	45E0000-45FFFFF	22F0000-22FFFFF
560	128 / 64	4600000-461FFFF	2300000-230FFFF
561	128 / 64	4620000-463FFFF	2310000-231FFFF
562	128 / 64	4640000-465FFFF	2320000-232FFFF
563	128 / 64	4660000-467FFFF	2330000-233FFFF
564	128 / 64	4680000-469FFFF	2340000-234FFFF
565	128 / 64	46A0000-46BFFFF	2350000-235FFFF
566	128 / 64	46C0000-46DFFFF	2360000-236FFFF
567	128 / 64	46E0000-46FFFFF	2370000-237FFFF
568	128 / 64	4700000-471FFFF	2380000-238FFFF
569	128 / 64	4720000-473FFFF	2390000-239FFFF
570	128 / 64	4740000-475FFFF	23A0000-23AFFFF
571	128 / 64	4760000-477FFFF	23B0000-23BFFFF
572	128 / 64	4780000-479FFFF	23C0000-23CFFFF
573	128 / 64	47A0000-47BFFFF	23D0000-23DFFFF
574	128 / 64	47C0000-47DFFFF	23E0000-23EFFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
575	128 / 64	47E0000-47FFFFF	23F0000-23FFFFF
576	128 / 64	4800000-481FFFF	2400000-240FFFF
577	128 / 64	4820000-483FFFF	2410000-241FFFF
578	128 / 64	4840000-485FFFF	2420000-242FFFF
579	128 / 64	4860000-487FFFF	2430000-243FFFF
580	128 / 64	4880000-489FFFF	2440000-244FFFF
581	128 / 64	48A0000-48BFFFF	2450000-245FFFF
582	128 / 64	48C0000-48DFFFF	2460000246FFFF
583	128 / 64	48E0000-48FFFFF	2470000-247FFFF
584	128 / 64	4900000-491FFFF	2480000-248FFFF
585	128 / 64	4920000-493FFFF	2490000-249FFFF
586	128 / 64	4940000-495FFFF	24A0000-24AFFFF
587	128 / 64	4960000-497FFFF	24B0000-24BFFFF
588	128 / 64	4980000-499FFFF	24C0000-24CFFFF
589	128 / 64	49A0000-49BFFFF	24D0000-24DFFFF
590	128 / 64	49C0000-49DFFFF	24E0000-24EFFFF
591	128 / 64	49E0000-49FFFFF	24F0000-24FFFFF
592	128 / 64	4A00000-4A1FFFF	2500000-250FFFF
593	128 / 64	4A20000-4A3FFFF	2510000-251FFFF
594	128 / 64	4A40000-4A5FFFF	2520000-252FFFF
595	128 / 64	4A60000-4A7FFFF	2530000-253FFFF
596	128 / 64	4A80000-4A9FFFF	2540000-254FFFF
597	128 / 64	4AA0000-4ABFFFF	2550000-255FFFF
598	128 / 64	4AC0000-4ADFFFF	2560000-256FFFF
599	128 / 64	4AE0000-4AFFFFF	2570000-257FFFF
600	128 / 64	4B00000-4B1FFFF	2580000-258FFFF
601	128 / 64	4B20000-4B3FFFF	2590000-259FFFF
602	128 / 64	4B40000-4B5FFFF	25A0000-25AFFFF
603	128 / 64	4B60000-4B7FFFF	25B0000-25BFFFF
604	128 / 64	4B80000-4B9FFFF	25C0000-25CFFFF
605	128 / 64	4BA0000-4BBFFFF	25D0000-25DFFFF
606	128 / 64	4BC0000-4BDFFFF	25E0000-25EFFFF
607	128 / 64	4BE0000-4BFFFFF	25F0000-25FFFFF
608	128 / 64	4C00000-4C1FFFF	2600000-260FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
609	128 / 64	4C20000-4C3FFFF	2610000-261FFFF
610	128 / 64	4C40000-4C5FFFF	2620000-262FFFF
611	128 / 64	4C60000-4C7FFFF	2630000-263FFFF
612	128 / 64	4C80000-4C9FFFF	2640000-264FFFF
613	128 / 64	4CA0000-4CBFFFF	2650000-265FFFF
614	128 / 64	4CC0000-4CDFFFF	2660000-266FFFF
615	128 / 64	4CE0000-4CFFFFF	2670000-267FFFF
616	128 / 64	4D00000-4D1FFFF	2680000-268FFFF
617	128 / 64	4D20000-4D3FFFF	2690000-269FFFF
618	128 / 64	4D40000-4D5FFFF	26A0000-26AFFFF
619	128 / 64	4D60000-4D7FFFF	26B0000-26BFFFF
620	128 / 64	4D80000-4D9FFFF	26C0000-26CFFFF
621	128 / 64	4DA0000-4DBFFFF	26D0000-26DFFFF
622	128 / 64	4DC0000-4DDFFFF	26E0000-26EFFFF
623	128 / 64	4DE0000-4DFFFFF	26F0000-26FFFFF
624	128 / 64	4E00000-4E1FFFF	2700000-270FFFF
625	128 / 64	4E20000-4E3FFFF	2710000-271FFFF
626	128 / 64	4E40000-4E5FFFF	2720000-272FFFF
627	128 / 64	4E60000-4E7FFFF	2730000-273FFFF
628	128 / 64	4E80000-4E9FFFF	2740000-274FFFF
629	128 / 64	4EA0000-4EBFFFF	2750000-275FFFF
630	128 / 64	4EC0000-4EDFFFF	2760000-276FFFF
631	128 / 64	4EE0000-4EFFFFF	2770000-277FFFF
632	128 / 64	4F00000-4F1FFFF	2780000-278FFFF
633	128 / 64	4F20000-4F3FFFF	2790000-279FFFF
634	128 / 64	4F40000-4F5FFFF	27A0000-27AFFFF
635	128 / 64	4F60000-4F7FFFF	27B0000-27BFFFF
636	128 / 64	4F80000-4F9FFFF	27C0000-27CFFFF
637	128 / 64	4FA0000-4FBFFFF	27D0000-27DFFFF
638	128 / 64	4FC0000-4FDFFFF	27E0000-27EFFFF
639	128 / 64	4FE0000-4FFFFFF	27F0000-27FFFFF
640	128 / 64	5000000-501FFFF	2800000-280FFFF
641	128 / 64	5020000-503FFFF	2810000-281FFFF
642	128 / 64	5040000-505FFFF	2820000-282FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
643	128 / 64	5060000-507FFFF	2830000-283FFFF
644	128 / 64	5080000-509FFFF	2840000-284FFFF
645	128 / 64	50A0000-50BFFFF	2850000-285FFFF
646	128 / 64	50C0000-50DFFFF	2860000-286FFFF
647	128 / 64	50E0000-50FFFFF	2870000-287FFFF
648	128 / 64	5100000-511FFFF	2880000-288FFFF
649	128 / 64	5120000-513FFFF	2890000-289FFFF
650	128 / 64	5140000-515FFFF	28A0000-28AFFFF
651	128 / 64	5160000-517FFFF	28B0000-28BFFFF
652	128 / 64	5180000-519FFFF	28C0000-28CFFFF
653	128 / 64	51A0000-51BFFFF	28D0000-28DFFFF
654	128 / 64	51C0000-51DFFFF	28E0000-28EFFFF
655	128 / 64	51E0000-51FFFFF	28F0000-28FFFFF
656	128 / 64	5200000-521FFFF	2900000-290FFFF
657	128 / 64	5220000-523FFFF	2910000-291FFFF
658	128 / 64	5240000-525FFFF	2920000-292FFFF
659	128 / 64	5260000-527FFFF	2930000-293FFFF
660	128 / 64	5280000-529FFFF	2940000-294FFFF
661	128 / 64	52A0000-52BFFFF	2950000-295FFFF
662	128 / 64	52C0000-52DFFFF	2960000-296FFFF
663	128 / 64	52E0000-52FFFFF	2970000-297FFFF
664	128 / 64	5300000-531FFFF	2980000-298FFFF
665	128 / 64	5320000-533FFFF	2990000-299FFFF
666	128 / 64	5340000-535FFFF	29A0000-29AFFFF
667	128 / 64	5360000-537FFFF	29B0000-29BFFFF
668	128 / 64	5380000-539FFFF	29C0000-29CFFFF
669	128 / 64	53A0000-53BFFFF	29D0000-29DFFFF
670	128 / 64	53C0000-53DFFFF	29E0000-29EFFFF
671	128 / 64	53E0000-53FFFFF	29F0000-29FFFFF
672	128 / 64	5400000-541FFFF	2A00000-2A0FFFF
673	128 / 64	5420000-543FFFF	2A10000-2A1FFFF
674	128 / 64	5440000-545FFFF	2A20000-2A2FFFF
675	128 / 64	5460000-547FFFF	2A30000-2A3FFFF
676	128 / 64	5480000-549FFFF	2A40000-2A4FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
677	128 / 64	54A0000-54BFFFF	2A50000-2A5FFFF
678	128 / 64	54C0000-54DFFFF	2A60000-2A6FFFF
679	128 / 64	54E0000-54FFFFF	2A70000-2A7FFFF
680	128 / 64	5500000-551FFFF	2A80000-2A8FFFF
681	128 / 64	5520000-553FFFF	2A90000-2A9FFFF
682	128 / 64	5540000-555FFFF	2AA0000-2AAFFFF
683	128 / 64	5560000-557FFFF	2AB0000-2ABFFFF
684	128 / 64	5580000-559FFFF	2AC0000-2ACFFFF
685	128 / 64	55A0000-55BFFFF	2AD0000-2ADFFFF
686	128 / 64	55C0000-55DFFFF	2AE0000-2AEFFFF
687	128 / 64	55E0000-55FFFFF	2AF0000-2AFFFFF
688	128 / 64	5600000-561FFFF	2B00000-2B0FFFF
689	128 / 64	5620000-563FFFF	2B10000-2B1FFFF
690	128 / 64	5640000-565FFFF	2B20000-2B2FFFF
691	128 / 64	5660000-567FFFF	2B30000-2B3FFFF
692	128 / 64	5680000-569FFFF	2B40000-2B4FFFF
693	128 / 64	56A0000-56BFFFF	2B50000-2B5FFFF
694	128 / 64	56C0000-56DFFFF	2B60000-2B6FFFF
695	128 / 64	56E0000-56FFFFF	2B70000-2B7FFFF
696	128 / 64	5700000-571FFFF	2B80000-2B8FFFF
697	128 / 64	5720000-573FFFF	2B90000-2B9FFFF
698	128 / 64	5740000-575FFFF	2BA0000-2BAFFFF
699	128 / 64	5760000-577FFFF	2BB0000-2BBFFFF
700	128 / 64	5780000-579FFFF	2BC0000-2BCFFFF
701	128 / 64	57A0000-57BFFFF	2BD0000-2BDFFFF
702	128 / 64	57C0000-57DFFFF	2BE0000-2BEFFFF
703	128 / 64	57E0000-57FFFFF	2BF0000-2BFFFFF
704	128 / 64	5800000-581FFFF	2C00000-2C0FFFF
705	128 / 64	5820000-583FFFF	2C10000-2C1FFFF
706	128 / 64	5840000-585FFFF	2C20000-2C2FFFF
707	128 / 64	5860000-587FFFF	2C30000-2C3FFFF
708	128 / 64	5880000-589FFFF	2C40000-2C4FFFF
709	128 / 64	58A0000-58BFFFF	2C50000-2C5FFFF
710	128 / 64	58C0000-58DFFFF	2C60000-2C6FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
711	128 / 64	58E0000-58FFFFF	2C70000-2C7FFFF
712	128 / 64	5900000-591FFFF	2C80000-2C8FFFF
713	128 / 64	5920000-593FFFF	2C90000-2C9FFFF
714	128 / 64	5940000-595FFFF	2CA0000-2CAFFFF
715	128 / 64	5960000-597FFFF	2CB0000-2CBFFFF
716	128 / 64	5980000-599FFFF	2CC0000-2CCFFFF
717	128 / 64	59A0000-59BFFFF	2CD0000-2CDFFFF
718	128 / 64	59C0000-59DFFFF	2CE0000-2CEFFFF
719	128 / 64	59E0000-59FFFFF	2CF0000-2CFFFFF
720	128 / 64	5A00000-5A1FFFF	2D00000-2D0FFFF
721	128 / 64	5A20000-5A3FFFF	2D10000-2D1FFFF
722	128 / 64	5A40000-5A5FFFF	2D20000-2D2FFFF
723	128 / 64	5A60000-5A7FFFF	2D30000-2D3FFFF
724	128 / 64	5A80000-5A9FFFF	2D40000-2D4FFFF
725	128 / 64	5AA0000-5ABFFFF	2D50000-2D5FFFF
726	128 / 64	5AC0000-5ADFFFF	2D60000-2D6FFFF
727	128 / 64	5AE0000-5AFFFFF	2D70000-2D7FFFF
728	128 / 64	5B00000-5B1FFFF	2D80000-2D8FFFF
729	128 / 64	5B20000-5B3FFFF	2D90000-2D9FFFF
730	128 / 64	5B40000-5B5FFFF	2DA0000-2DAFFFF
731	128 / 64	5B60000-5B7FFFF	2DB0000-2DBFFFF
732	128 / 64	5B80000-5B9FFFF	2DC0000-2DCFFFF
733	128 / 64	5BA0000-5BBFFFF	2DD0000-2DDFFFF
734	128 / 64	5BC0000-5BDFFFF	2DE0000-2DEFFFF
735	128 / 64	5BE0000-5BFFFFF	2DF0000-2DFFFFF
736	128 / 64	5C00000-5C1FFFF	2E00000-2E0FFFF
737	128 / 64	5C20000-5C3FFFF	2E10000-2E1FFFF
738	128 / 64	5C40000-5C5FFFF	2E20000-2E2FFFF
739	128 / 64	5C60000-5C7FFFF	2E30000-2E3FFFF
740	128 / 64	5C80000-5C9FFFF	2E40000-2E4FFFF
741	128 / 64	5CA0000-5CBFFFF	2E50000-2E5FFFF
742	128 / 64	5CC0000-5CDFFFF	2E60000-2E6FFFF
743	128 / 64	5CE0000-5CFFFFF	2E70000-2E7FFFF
744	128 / 64	5D00000-5D1FFFF	2E80000-2E8FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
745	128 / 64	5D20000-5D3FFFF	2E90000-2E9FFFF
746	128 / 64	5D40000-5D5FFFF	2EA0000-2EAFFFF
747	128 / 64	5D60000-5D7FFFF	2EB0000-2EBFFFF
748	128 / 64	5D80000-5D9FFFF	2EC0000-2ECFFFF
749	128 / 64	5DA0000-5DBFFFF	2ED0000-2EDFFFF
750	128 / 64	5DC0000-5DDFFFF	2EE0000-2EEFFFF
751	128 / 64	5DE0000-5DFFFFF	2EF0000-2EFFFFF
752	128 / 64	5E00000-5E1FFFF	2F00000-2F0FFFF
753	128 / 64	5E20000-5E3FFFF	2F10000-2F1FFFF
754	128 / 64	5E40000-5E5FFFF	2F20000-2F2FFFF
755	128 / 64	5E60000-5E7FFFF	2F30000-2F3FFFF
756	128 / 64	5E80000-5E9FFFF	2F40000-2F4FFFF
757	128 / 64	5EA0000-5EBFFFF	2F50000-2F5FFFF
758	128 / 64	5EC0000-5EDFFFF	2F60000-2F6FFFF
759	128 / 64	5EE0000-5EFFFFF	2F70000-2F7FFFF
760	128 / 64	5F00000-5F1FFFF	2F80000-2F8FFFF
761	128 / 64	5F20000-5F3FFFF	2F90000-2F9FFFF
762	128 / 64	5F40000-5F5FFFF	22FA00002FAFFFF
763	128 / 64	5F60000-5F7FFFF	2FB0000-2FBFFFF
764	128 / 64	5F80000-5F9FFFF	2FC0000-2FCFFFF
765	128 / 64	5FA0000-5FBFFFF	2FD0000-2FDFFFF
766	128 / 64	5FC0000-5FDFFFF	2FE0000-2FEFFFF
767	128 / 64	5FE0000-5FFFFFF	2FF0000-2FFFFFF
768	128 / 64	6000000-601FFFF	3000000-300FFFF
769	128 / 64	6020000-603FFFF	3010000-301FFFF
770	128 / 64	6040000-605FFFF	3020000-302FFFF
771	128 / 64	6060000-607FFFF	3030000-303FFFF
772	128 / 64	6080000-609FFFF	3040000-304FFFF
773	128 / 64	60A0000-60BFFFF	3050000-305FFFF
774	128 / 64	60C0000-60DFFFF	3060000-306FFFF
775	128 / 64	60E0000-60FFFFF	3070000-307FFFF
776	128 / 64	6100000-611FFFF	3080000-308FFFF
777	128 / 64	6120000-613FFFF	3090000-309FFFF
778	128 / 64	6140000-615FFFF	30A0000-30AFFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
779	128 / 64	6160000-617FFFF	30B0000-30BFFFF
780	128 / 64	6180000-619FFFF	30C0000-30CFFFF
781	128 / 64	61A0000-61BFFFF	30D0000-30DFFFF
782	128 / 64	61C0000-61DFFFF	30E0000-30EFFFF
783	128 / 64	61E0000-61FFFFF	30F0000-30FFFFF
784	128 / 64	6200000-621FFFF	3100000-310FFFF
785	128 / 64	6220000-623FFFF	3110000-311FFFF
786	128 / 64	6240000-625FFFF	3120000-312FFFF
787	128 / 64	6260000-627FFFF	3130000-313FFFF
788	128 / 64	6280000-629FFFF	3140000-314FFFF
789	128 / 64	62A0000-62BFFFF	3150000-315FFFF
790	128 / 64	62C0000-62DFFFF	3160000-316FFFF
791	128 / 64	62E0000-62FFFFF	3170000-317FFFF
792	128 / 64	6300000-631FFFF	3180000-318FFFF
793	128 / 64	6320000-633FFFF	3190000-319FFFF
794	128 / 64	6340000-635FFFF	31A0000-31AFFFF
795	128 / 64	6360000-637FFFF	31B0000-31BFFFF
796	128 / 64	6380000-639FFFF	31C0000-31CFFFF
797	128 / 64	63A0000-63BFFFF	31D0000-31DFFFF
798	128 / 64	63C0000-63DFFFF	31E0000-31EFFFF
799	128 / 64	63E0000-63FFFFF	31F0000-31FFFFF
800	128 / 64	6400000-641FFFF	3200000-320FFFF
801	128 / 64	6420000-643FFFF	3210000-321FFFF
802	128 / 64	6440000-645FFFF	3220000-322FFFF
803	128 / 64	6460000-647FFFF	3230000-323FFFF
804	128 / 64	6480000-649FFFF	3240000-324FFFF
805	128 / 64	64A0000-64BFFFF	3250000-325FFFF
806	128 / 64	64C0000-64DFFFF	3260000-326FFFF
807	128 / 64	64E0000-64FFFFF	3270000-327FFFF
808	128 / 64	6500000-651FFFF	3280000-328FFFF
809	128 / 64	6520000-653FFFF	3290000-329FFFF
810	128 / 64	6540000-655FFFF	32A0000-32AFFFF
811	128 / 64	6560000-657FFFF	32B0000-32BFFFF
812	128 / 64	6580000-659FFFF	32C0000-32CFFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
813	128 / 64	65A0000-65BFFFF	32D0000-32DFFFF
814	128 / 64	65C0000-65DFFFF	32E0000-32EFFFF
815	128 / 64	65E0000-65FFFFF	32F0000-32FFFFF
816	128 / 64	6600000-661FFFF	3300000-330FFFF
817	128 / 64	6620000-663FFFF	3310000-331FFFF
818	128 / 64	6640000-665FFFF	3320000-332FFFF
819	128 / 64	6660000-667FFFF	3330000-333FFFF
820	128 / 64	6680000-669FFFF	3340000-334FFFF
821	128 / 64	66A0000-66BFFFF	3350000-335FFFF
822	128 / 64	66C0000-66DFFFF	3360000-336FFFF
823	128 / 64	66E0000-66FFFFF	3370000-337FFFF
824	128 / 64	6700000-671FFFF	3380000-338FFFF
825	128 / 64	6720000-673FFFF	3390000-339FFFF
826	128 / 64	6740000-675FFFF	33A0000-33AFFFF
827	128 / 64	6760000-677FFFF	33B0000-33BFFFF
828	128 / 64	6780000-679FFFF	33C0000-33CFFFF
829	128 / 64	67A0000-67BFFFF	33D0000-33DFFFF
830	128 / 64	67C0000-67DFFFF	33E0000-33EFFFF
831	128 / 64	67E0000-67FFFFF	33F0000-33FFFFF
832	128 / 64	6800000-681FFFF	3400000-340FFFF
833	128 / 64	6820000-683FFFF	3410000-341FFFF
834	128 / 64	6840000-685FFFF	3420000-342FFFF
835	128 / 64	6860000-687FFFF	3430000-343FFFF
836	128 / 64	6880000-689FFFF	3440000-344FFFF
837	128 / 64	68A0000-68BFFFF	3450000-345FFFF
838	128 / 64	68C0000-68DFFFF	3460000-346FFFF
839	128 / 64	68E0000-68FFFFF	3470000-347FFFF
840	128 / 64	6900000-691FFFF	3480000-348FFFF
841	128 / 64	6920000-693FFFF	3490000-349FFFF
842	128 / 64	6940000-695FFFF	34A0000-34AFFFF
843	128 / 64	6960000-697FFFF	34B0000-34BFFFF
844	128 / 64	6980000-699FFFF	34C0000-34CFFFF
845	128 / 64	69A0000-69BFFFF	34D0000-34DFFFF
846	128 / 64	69C0000-69DFFFF	34E0000-34EFFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
847	128 / 64	69E0000-69FFFFF	34F0000-34FFFFF
848	128 / 64	6A00000-6A1FFFF	3500000-350FFFF
849	128 / 64	6A20000-6A3FFFF	3510000-351FFFF
850	128 / 64	6A40000-6A5FFFF	3520000-352FFFF
851	128 / 64	6A60000-6A7FFFF	3530000-353FFFF
852	128 / 64	6A80000-6A9FFFF	3540000-354FFFF
853	128 / 64	6AA0000-6ABFFFF	3550000-355FFFF
854	128 / 64	6AC0000-6ADFFFF	3560000-356FFFF
855	128 / 64	6AE0000-6AFFFFF	3570000-357FFFF
856	128 / 64	6B00000-6B1FFFF	3580000-358FFFF
857	128 / 64	6B20000-6B3FFFF	3590000-359FFFF
858	128 / 64	6B40000-6B5FFFF	35A0000-35AFFFF
859	128 / 64	6B60000-6B7FFFF	35B0000-35BFFFF
860	128 / 64	6B80000-6B9FFFF	35C0000-35CFFFF
861	128 / 64	6BA0000-6BBFFFF	35D0000-35DFFFF
862	128 / 64	6BC0000-6BDFFFF	35E0000-35EFFFF
863	128 / 64	6BE0000-6BFFFFF	35F0000-35FFFFF
864	128 / 64	6C00000-6C1FFFF	3600000-360FFFF
865	128 / 64	6C20000-6C3FFFF	3610000-361FFFF
866	128 / 64	6C40000-6C5FFFF	3620000-362FFFF
867	128 / 64	6C60000-6C7FFFF	3630000-363FFFF
868	128 / 64	6C80000-6C9FFFF	3640000-364FFFF
869	128 / 64	6CA0000-6CBFFFF	3650000-365FFFF
870	128 / 64	6CC0000-6CDFFFF	3660000-366FFFF
871	128 / 64	6CE0000-6CFFFFF	3670000-367FFFF
872	128 / 64	6D00000-6D1FFFF	3680000-368FFFF
873	128 / 64	6D20000-6D3FFFF	3690000-369FFFF
874	128 / 64	6D40000-6D5FFFF	36A0000-36AFFFF
875	128 / 64	6D60000-6D7FFFF	36B0000-36BFFFF
876	128 / 64	6D80000-6D9FFFF	36C0000-36CFFFF
877	128 / 64	6DA0000-6DBFFFF	36D0000-36DFFFF
878	128 / 64	6DC0000-6DDFFFF	36E0000-36EFFFF
879	128 / 64	6DE0000-6DFFFFF	36F0000-36FFFFF
880	128 / 64	6E00000-6E1FFFF	3700000-370FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
881	128 / 64	6E20000-6E3FFFF	3710000-371FFFF
882	128 / 64	6E40000-6E5FFFF	3720000-372FFFF
883	128 / 64	6E60000-6E7FFFF	3730000-373FFFF
884	128 / 64	6E80000-6E9FFFF	3740000-374FFFF
885	128 / 64	6EA0000-6EBFFFF	3750000-375FFFF
886	128 / 64	6EC0000-6EDFFFF	3760000-376FFFF
887	128 / 64	6EE0000-6EFFFFF	3770000-377FFFF
888	128 / 64	6F00000-6F1FFFF	3780000-378FFFF
889	128 / 64	6F20000-6F3FFFF	3790000-379FFFF
890	128 / 64	6F40000-6F5FFFF	37A0000-37AFFFF
891	128 / 64	6F60000-6F7FFFF	37B0000-37BFFFF
892	128 / 64	6F80000-6F9FFFF	37C0000-37CFFFF
893	128 / 64	6FA0000-6FBFFFF	37D0000-37DFFFF
894	128 / 64	6FC0000-6FDFFFF	37E0000-37EFFFF
895	128 / 64	6FE0000-6FFFFFF	37F0000-37FFFFF
896	128 / 64	7000000-701FFFF	3800000-380FFFF
897	128 / 64	7020000-703FFFF	3810000-381FFFF
898	128 / 64	7040000-705FFFF	3820000-382FFFF
899	128 / 64	7060000-707FFFF	3830000-383FFFF
900	128 / 64	7080000-709FFFF	3840000-384FFFF
901	128 / 64	70A0000-70BFFFF	3850000-385FFFF
902	128 / 64	70C0000-70DFFFF	3860000-386FFFF
903	128 / 64	70E0000-70FFFFF	3870000-387FFFF
904	128 / 64	7100000-711FFFF	3880000-388FFFF
905	128 / 64	7120000-713FFFF	3890000-389FFFF
906	128 / 64	7140000-715FFFF	38A0000-38AFFFF
907	128 / 64	7160000-717FFFF	38B0000-38BFFFF
908	128 / 64	7180000-719FFFF	38C0000-38CFFFF
909	128 / 64	71A0000-71BFFFF	38D0000-38DFFFF
910	128 / 64	71C0000-71DFFFF	38E0000-38EFFFF
911	128 / 64	71E0000-71FFFFF	38F0000-38FFFFF
912	128 / 64	7200000-721FFFF	3900000-390FFFF
913	128 / 64	7220000-723FFFF	3910000-391FFFF
914	128 / 64	7240000-725FFFF	3920000-392FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
915	128 / 64	7260000-727FFFF	3930000-393FFFF
916	128 / 64	7280000-729FFFF	3940000-394FFFF
917	128 / 64	72A0000-72BFFFF	3950000-395FFFF
918	128 / 64	72C0000-72DFFFF	3960000-396FFFF
919	128 / 64	72E0000-72FFFFF	3970000-397FFFF
920	128 / 64	7300000-731FFFF	3980000-398FFFF
921	128 / 64	7320000-733FFFF	3990000-399FFFF
922	128 / 64	7340000-735FFFF	39A0000-39AFFFF
923	128 / 64	7360000-737FFFF	39B0000-39BFFFF
924	128 / 64	7380000-739FFFF	39C0000-39CFFFF
925	128 / 64	73A0000-73BFFFF	39D0000-39DFFFF
926	128 / 64	73C0000-73DFFFF	39E0000-39EFFFF
927	128 / 64	73E0000-73FFFFF	39F0000-39FFFFF
928	128 / 64	7400000-741FFFF	3A00000-3A0FFFF
929	128 / 64	7420000-743FFFF	3A10000-3A1FFFF
930	128 / 64	7440000-745FFFF	3A20000-3A2FFFF
931	128 / 64	7460000-747FFFF	3A30000-3A3FFFF
932	128 / 64	7480000-749FFFF	3A40000-3A4FFFF
933	128 / 64	74A0000-74BFFFF	3A50000-3A5FFFF
934	128 / 64	74C0000-74DFFFF	3A60000-3A6FFFF
935	128 / 64	74E0000-74FFFFF	3A70000-3A7FFFF
936	128 / 64	7500000-751FFFF	3A80000-3A8FFFF
937	128 / 64	7520000-753FFFF	3A90000-3A9FFFF
938	128 / 64	7540000-755FFFF	3AA0000-3AAFFFF
939	128 / 64	7560000-757FFFF	3AB0000-3ABFFFF
940	128 / 64	7580000-759FFFF	3AC0000-3ACFFFF
941	128 / 64	75A0000-75BFFFF	3AD0000-3ADFFFF
942	128 / 64	75C0000-75DFFFF	3AE0000-3AEFFFF
943	128 / 64	75E0000-75FFFFF	3AF0000-3AFFFFF
944	128 / 64	7600000-761FFFF	3B00000-3B0FFFF
945	128 / 64	7620000-763FFFF	3B10000-3B1FFFF
946	128 / 64	7640000-765FFFF	3B20000-3B2FFFF
947	128 / 64	7660000-767FFFF	3B30000-3B3FFFF
948	128 / 64	7680000-769FFFF	3B40000-3B4FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
949	128 / 64	76A0000-76BFFFF	3B50000-3B5FFFF
950	128 / 64	76C0000-76DFFFF	3B60000-3B6FFFF
951	128 / 64	76E0000-76FFFFF	3B70000-3B7FFFF
952	128 / 64	7700000-771FFFF	3B80000-3B8FFFF
953	128 / 64	7720000-773FFFF	3B90000-3B9FFFF
954	128 / 64	7740000-775FFFF	3BA0000-3BAFFFF
955	128 / 64	7760000-777FFFF	3BB0000-3BBFFFF
956	128 / 64	7780000-779FFFF	3BC0000-3BCFFFF
957	128 / 64	77A0000-77BFFFF	3BD0000-3BDFFFF
958	128 / 64	77C0000-77DFFFF	3BE0000-3BEFFFF
959	128 / 64	77E0000-77FFFFF	3BF0000-3BFFFFF
960	128 / 64	7800000-781FFFF	3C00000-3C0FFFF
961	128 / 64	7820000-783FFFF	3C10000-3C1FFFF
962	128 / 64	7840000-785FFFF	3C20000-3C2FFFF
963	128 / 64	7860000-787FFFF	3C30000-3C3FFFF
964	128 / 64	7880000-789FFFF	3C40000-3C4FFFF
965	128 / 64	78A0000-78BFFFF	3C50000-3C5FFFF
966	128 / 64	78C0000-78DFFFF	3C60000-3C6FFFF
967	128 / 64	78E0000-78FFFFF	3C70000-3C7FFFF
968	128 / 64	7900000-791FFFF	3C80000-3C8FFFF
969	128 / 64	7920000-793FFFF	3C90000-3C9FFFF
970	128 / 64	7940000-795FFFF	3CA0000-3CAFFFF
971	128 / 64	7960000-797FFFF	3CB0000-3CBFFFF
972	128 / 64	7980000-799FFFF	3CC0000-3CCFFFF
973	128 / 64	79A0000-79BFFFF	3CD0000-3CDFFFF
974	128 / 64	79C0000-79DFFFF	3CE0000-3CEFFFF
975	128 / 64	79E0000-79FFFFF	3CF0000-3CFFFFF
976	128 / 64	7A00000-7A1FFFF	3D00000-3D0FFFF
977	128 / 64	7A20000-7A3FFFF	3D10000-3D1FFFF
978	128 / 64	7A40000-7A5FFFF	3D20000-3D2FFFF
979	128 / 64	7A60000-7A7FFFF	3D30000-3D3FFFF
980	128 / 64	7A80000-7A9FFFF	3D40000-3D4FFFF
981	128 / 64	7AA0000-7ABFFFF	3D50000-3D5FFFF
982	128 / 64	7AC0000-7ADFFFF	3D60000-3D6FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)[1][2][3][4]

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
983	128 / 64	7AE0000-7AFFFFF	3D70000-3D7FFFF
984	128 / 64	7B00000-7B1FFFF	3D80000-3D8FFFF
985	128 / 64	7B20000-7B3FFFF	3D90000-3D9FFFF
986	128 / 64	7B40000-7B5FFFF	3DA0000-3DAFFFF
987	128 / 64	7B60000-7B7FFFF	3DB0000-3DBFFFF
988	128 / 64	7B80000-7B9FFFF	3DC0000-3DCFFFF
989	128 / 64	7BA0000-7BBFFFF	3DD0000-3DDFFFF
990	128 / 64	7BC0000-7BDFFFF	3DE0000-3DEFFFF
991	128 / 64	7BE0000-7BFFFFF	3DF0000-3DFFFFF
992	128 / 64	7C00000-7C1FFFF	3E00000-3E0FFFF
993	128 / 64	7C20000-7C3FFFF	3E10000-3E1FFFF
994	128 / 64	7C40000-7C5FFFF	3E20000-3E2FFFF
995	128 / 64	7C60000-7C7FFFF	3E30000-3E3FFFF
996	128 / 64	7C80000-7C9FFFF	3E40000-3E4FFFF
997	128 / 64	7CA0000-7CBFFFF	3E50000-3E5FFFF
998	128 / 64	7CC0000-7CDFFFF	3E60000-3E6FFFF
999	128 / 64	7CE0000-7CFFFFF	3E70000-3E7FFFF
1000	128 / 64	7D00000-7D1FFFF	3E80000-3E8FFFF
1001	128 / 64	7D20000-7D3FFFF	3E90000-3E9FFFF
1002	128 / 64	7D40000-7D5FFFF	3EA0000-3EAFFFF
1003	128 / 64	7D60000-7D7FFFF	3EB0000-3EBFFFF
1004	128 / 64	7D80000-7D9FFFF	3EC0000-3ECFFFF
1005	128 / 64	7DA0000-7DBFFFF	3ED0000-3EDFFFF
1006	128 / 64	7DC0000-7DDFFFF	3EE0000-3EEFFFF
1007	128 / 64	7DE0000-7DFFFFF	3EF0000-3EFFFFF
1008	128 / 64	7E00000-7E1FFFF	3F00000-3F0FFFF
1009	128 / 64	7E20000-7E3FFFF	3F10000-3F1FFFF
1010	128 / 64	7E40000-7E5FFFF	3F20000-3F2FFFF
1011	128 / 64	7E60000-7E7FFFF	3F30000-3F3FFFF
1012	128 / 64	7E80000-7E9FFFF	3F40000-3F4FFFF
1013	128 / 64	7EA0000-7EBFFFF	3F50000-3F5FFFF
1014	128 / 64	7EC0000-7EDFFFF	3F60000-3F6FFFF
1015	128 / 64	7EE0000-7EFFFFF	3F70000-3F7FFFF
1016	128 / 64	7F00000-7F1FFFF	3F80000-3F8FFFF

Table 33. Block Address Table for Descrete Device (Up to 1-Gbit)(1)(2)(3)(4)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
1017	128 / 64	7F20000-7F3FFFF	3F90000-3F9FFFF
1018	128 / 64	7F40000-7F5FFFF	3FA0000-3FAFFFF
1019	128 / 64	7F60000-7F7FFFF	3FB0000-3FBFFFF
1020	128 / 64	7F80000-7F9FFFF	3FC0000-3FCFFFF
1021	128 / 64	7FA0000-7FBFFFF	3FD0000-3FDFFFF
1022	128 / 64	7FC0000-7FDFFFF	3FE0000-3FEFFFF
1023	128 / 64	7FE0000-7FFFFFF	3FF0000-3FFFFFF

1. The 256-Mbit device consists of 256 blocks, from block 0 to block 255.
2. The 512-Mbit device consists of 512 blocks, from block 0 to block 511.
3. The 1-Gbit device consists of 1024 blocks, from block 0 to block 1023.
4. The 2-Gbit device is a 1-Gbit/1-Gbit stack; there're in total 2048 blocks, from block 0 to block 2047, including upper die and bottom die.

Appendix B Common Flash Interface (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query command is issued, the memory enters Read CFI Query mode and read operations output the CFI data. *Table 34*, *Table 35*, *Table 36*, *Table 37* and *Table 38* and show the addresses (A-1, A0-A7) used to retrieve the data.

Table 34. Query structure overview(1)

Address		Sub-section name	Description
x16	x8		
10h	20h	CFI query identification string	Command set ID and algorithm data offset
1Bh	36h	System interface information	Device timing & voltage information
27h	4Eh	Device geometry definition	Flash device layout
40h	80h	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)

1. Query data are always presented on the lowest order data outputs.

Table 35. CFI query identification string(1)

Address		Data	Description	Value
x16	x8			
10h	20h	0051h	Query Unique ASCII String ‘QRY’	‘Q’
11h	22h	0052h		‘R’
12h	24h	0059h		‘Y’
13h	26h	0002h	Primary algorithm command set and control interface ID code 16 bit ID code defining a specific algorithm	AMD compatible
14h	28h	0000h		
15h	2Ah	0040h	Address for primary algorithm extended query table (see *Table 38*)	P = 40h
16h	2Ch	0000h		
17h	2Eh	0000h	Alternate vendor command set and control interface ID code second vendor - specified algorithm supported	NA
18h	30h	0000h		
19h	32h	0000h	Address for alternate algorithm extended query table	NA
1Ah	34h	0000h		

1. Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 36. CFI query system interface information(1)

Address		Data	Description	Value
x16	x8			
1Bh	36h	0027h	V_{CC} logic supply minimum Program/Erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	2.7 V
1Ch	38h	0036h	V_{CC} logic supply maximum Program/Erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	3.6 V
1Dh	3Ah	00B5h	V_{PPH} [programming] supply minimum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 mV	11.5 V
1Eh	3Ch	00C5h	V_{PPH} [programming] supply maximum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 10 mV	12.5 V
1Fh	3Eh	0009h	Typical time-out for single byte/word program = 2^n µs	512 µs
20h	40h	000Ah	Typical time-out for maximum size buffer program = 2^n µs	1024 µs
21h	42h	000Ah	Typical time-out for individual block erase = 2^n ms	1 s
22h	44h	0012h / 0013h / 0014h / 0015h	Typical time-out for full Chip Erase = 2^n ms	256-Mbit 262 s 512-Mbit 524 s 1-Gbit 1048 s 2-Gbit 2097 s
23h	46h	0001h	Maximum time-out for byte/word program = 2^n times typical time-out	1024 µs
24h	48h	0002h	Maximum time-out for buffer program = 2^n times typical time-out	4096 µs
25h	4Ah	0002h	Maximum time-out per individual block erase = 2^n times typical time-out	4 s
26h	4Ch	0002h	Maximum time-out for Chip Erase = 2^n times typical time-out	256-Mbit 1048 s 512-Mbit 2096 s 1-Gbit 4194 s 2-Gbit 8388 s

1. The values given in the above table are valid for both packages.

Table 37. Device geometry definition

Address		Data	Description	Value
x16	x8			
27h	4Eh	0019h / 001Ah / 001Bh/001Ch	Device size = 2^n in number of bytes	32 Mbytes 64 Mbytes 128 Mbytes 256 Mbytes
28h 29h	50h 52h	0002h 0000h	Flash device interface code description	x8, x16 Async.
2Ah 2Bh	54h 56h	000Ah 0000h	Maximum number of bytes in multiple-byte program or page= 2^n	1024
2Ch	58h	0001h	Number of Erase block regions. It specifies the number of regions containing contiguous Erase blocks of the same size.	1
2Dh 2Eh	5Ah 5Ch	00FFh / 00FFh / 00FFh / 00FFh 0000h / 0001h / 0003h / 0007h	Erase block region 1 information Number of Erase blocks of identical size = 00FFh + 1 / 01FFh +1 / 03FFh + 1	256 512 1024 2048
2Fh 30h	5Eh 60h	0000h 0002h	Erase block region 1 information Block size in region 1 = 0200h * 256 byte	128 Kbytes
31h 32h 33h 34h	62h 64h 66h 68h	0000h 0000h 0000h 0000h	Erase block region 2 information	0
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase block region 3 information	0
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase block region 4 information	0

Table 38. Primary algorithm-specific extended query table (1)

Address		Data	Description	Value
x16	x8			
40h	80h	0050h	Primary algorithm extended query table unique ASCII string “PRI”	‘P’
41h	82h	0052h		‘R’
42h	84h	0049h		‘I’
43h	86h	0031h	Major version number, ASCII	‘1’
44h	88h	0033h	Minor version number, ASCII	‘3’
45h	8Ah	0018h	Address sensitive unlock (bits 1 to 0) 00 = required, 01= not required Silicon revision number (bits 7 to 2)	Required
46h	8Ch	0002h	Erase Suspend 00 = not supported, 01 = Read only, 02 = read and write	2
47h	8Eh	0001h	Block protection 00 = not supported, x = number of blocks per group	1
48h	90h	0000h	Temporary block unprotect 00 = not supported, 01 = supported	Not supported
49h	92h	0008h	Block protect / unprotect 08 = M29EWH/M29EWL	8
4Ah	94h	0000h	Simultaneous operations: not supported	NA
4Bh	96h	0000h	Burst mode, 00 = not supported, 01 = supported	Not supported
4Ch	98h	0003h	Page mode, 00 = not supported, 01 = 8-word page 02 = 8-word page, 03 = 16-word page	16-word page
4Dh	9Ah	00B5h	V_{PPH} supply minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.5 V
4Eh	9Ch	00C5h	V_{PPH} supply maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.5 V
4Fh	9Eh	00xxh	Top/bottom boot block flag xx = 04h: Uniform device, HW protection for lowest block xx = 05h: Uniform device, HW protection for highest block	Uniform + V_{PP}/WP# protecting highest or lowest block
50h	A0h	0001h	Program suspend, 00 = not supported, 01 = supported	Supported

1. The values given in the above table are valid for both packages.

Appendix C Extended Memory Block

The M29EW has an extra block, the Extended Memory Block, that can be accessed using a dedicated command. This Extended Memory Block is 128words in x16 mode and 256bytes in x8 mode. It is used as a security block (to provide a permanent security identification number) or to store additional information.

The device can be shipped either with the Extended Memory Block pre-locked by Numonyx, or unlocked.

If the Extended Memory Block is not pre-locked by Numonyx, it can be customer-lockable. Its status is indicated by bit DQ7 of Extended Memory Block Verify Indicator. This bit is permanently set to either ‘1’ or ‘0’ at the Numonyx factory and cannot be changed. When set to ‘1’, it indicates that the device is pre-locked by Numonyx and the Extended Memory Block is protected. When set to ‘0’, it indicates that the device is customer-lockable. Bit DQ7 being permanently locked to either ‘1’ or ‘0’ is another security feature which ensures that a customer-lockable device cannot be used instead of a Numonyx pre-locked one.

Bit DQ7 is the most significant bit in the Extended Memory Block Verify Indicator. It can be read in Auto Select mode using either the Programmer (see *Table 7* and *Table 8*) or the In-system method (see *Table 9* and *Table 10*).

The Extended Memory Block can only be accessed when the device is in Extended Memory Block mode. For details of how the Extended Memory Block mode is entered and exited, refer to the *Section 6.3.1: Enter Extended Memory Block command* and *Section 6.3.2: Exit Extended Memory Block command*, and to *Table 13* and *Table 9*.

C.1 Numonyx pre-locked Extended Memory Block

If devices of which the Extended Memory Block is pre-locked upon customer request, the 128bits security identification number is written to the Extended Memory Block address space (see *Table 39: Extended Memory Block address and data*) in Numonyx factory. The contents in the Extended Memory Block cannot be changed any more.

C.2 Customer-lockable Extended Memory Block

A device where the Extended Memory Block is customer-lockable is delivered with the DQ7 bit set to ‘0’ and the Extended Memory Block unprotected. It is up to the customer to program and protect the Extended Memory Block but care must be taken because the protection of the Extended Memory Block is not reversible.

If the device has not been shipped with the Extended Memory Block pre-protected, the block can be protected by setting the Extended Memory Block Protection bit, DQ0, to ‘0’.

However, this bit can only be programmed once; and once it is protected the Extended Memory Block cannot be unprotected.

Once the Extended Memory Block is programmed, the Exit Extended Memory Block command must be issued to exit the Extended Memory Block mode and return the device to Read mode.

Table 39. Extended Memory Block address and data

Address[1]		Data		
x8	x16	Numonyx pre-locked	Customer-lockable	
000000h-00000Fh	000000h-000007h	Secure identification number	Determined by customers	Secure identification number
000010h-0000FFh	000008h-00007Fh	Protected and unavailable		Determined by customers

Appendix D Revision History

Table 40. Document revision history

Date	Version	Changes
May 2008	01	Initial release
Oct 2008	02	Update t_{AVAV} values in *Table 24* and *Table 25* Move buffer program flow chart to Chapter 6.2.1, as *Figure 7* Minor wording changes
Dec 2008	03	Apply Axcell™ as M29EW's branding name Change the names of timing parameters in *Table 20*, *Table 26* and *Table 27* Modify many waveforms to align the signal names Some wording changes Spec change of t_{EHEL2} from 20ns to 30ns, in *Table 27* Remove "Numonyx Confidential" Remove conventions section and set Revision History as *Appendix D* Update physical dimension information in *Table 29* Add Document Number Add 1-Gbit and 512-Mbit information into the data sheet Correct some typo error
Mar 2009	04	Correct the buffer write cycle numbers and wording correction in *Table 11* and *Table 12* Fix a text corruption in *Figure 7* Remove invalid ship options in *Chapter 5.1* Add *Figure 6* to explain the buffer programming Add buffer write misalignment description to better explain buffer programming usage in *Chapter 6.2.1* Move the disclaimer to the end of the data sheet Add 10Kohm pull-up resistor description for RY/BY# pin Update Fortified BGA physical dimension of ball size *Table 30*
Apr 2009	05	Remove notes about Enhanced Buffer Programming in *Chapter 6.2.2* Change V_{PPH} spec in *Table 18* and *Table 19* Change the address for VPB read in *Table 13* and *Table 14* Correct the DQ2 toggling states in *Table 17*
Jun 2009	06	Add technology information in cover page and *Chapter 1* Add RoHS and Halogen Free information in cover page Add block address information in *Chapter Appendix A* Move programming and erase performance as separate chapter in *Chapter 10* Add leaded, RoHS, halogen free information in *Chapter 12*
Oct 2009	07	Add 2-Gbit (1-Gbit/1-Gbit) stack device related information

Date	Version	Changes
Feb 2010	08	Revised part numbers in the *Table 32.: Valid Combinations of M29EW Part Numbers*. Update programming performance specifications and suspend latency specifications in *Table 28: Programming and Erase Performance* Update CFI information of program max timeout in *Table 36: CFI query system interface information* Add Erase to Suspend specification in *Table 28: Programming and Erase Performance* Add note for tDVWH in *Table 24: Write AC characteristics, Write Enable Controlled* Add note for tDVEH in *Table 25: Write AC characteristics, Chip Enable Controlled*
Apr 2010	09	Update JEDEC compliance in cover page Correct the buffer programming boundary limitation in *Section 6.2.1: Write to Buffer Program command* Update the specification of t_{PLRH}(t_{READY}) in *Table 26: Reset AC characteristics* Update the description of V_{PP}/WP# pin in *Chapter 2.8: V_{PP}/Write Protect (V_{PP}/WP#)* Add BYTE# transition waveform as *Figure 18: BYTE# Transition AC Waveform*
May 2010	10	Update the Random Read AC waveforms about BYTE# pin in *Section 9: DC and AC Parameters* Put a link for product part numbers in *Section 12: Ordering Information*

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